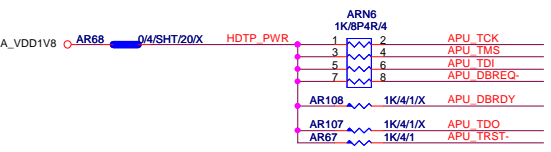
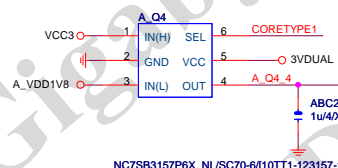
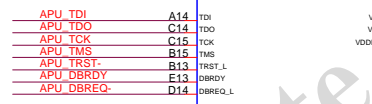


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

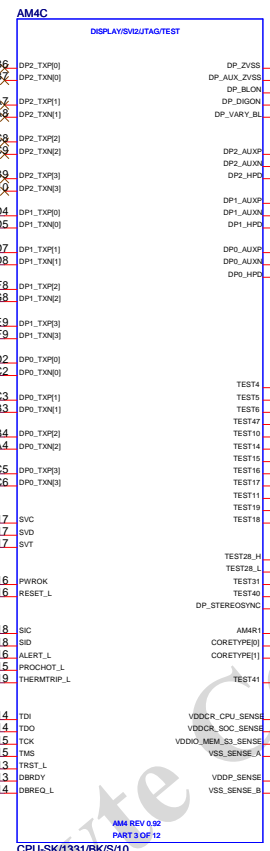


DVI

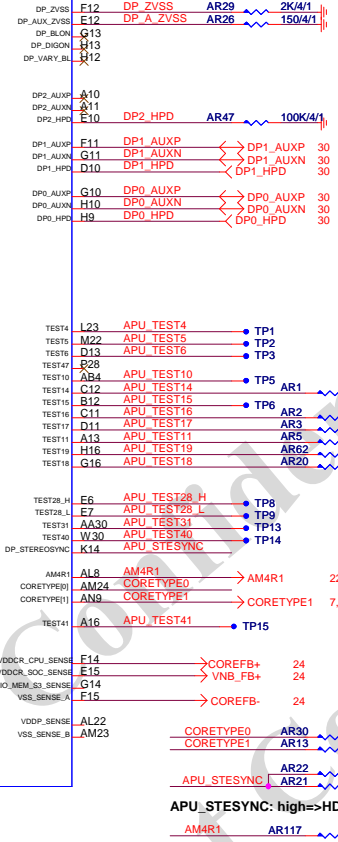
HDMI



NC7SB3157P6X_NL/SC70-6[10T11-123157-10R]



Placed within 1500 mils from APU



APU_STESYNC: high=>HDMI, low=>NO HDMI



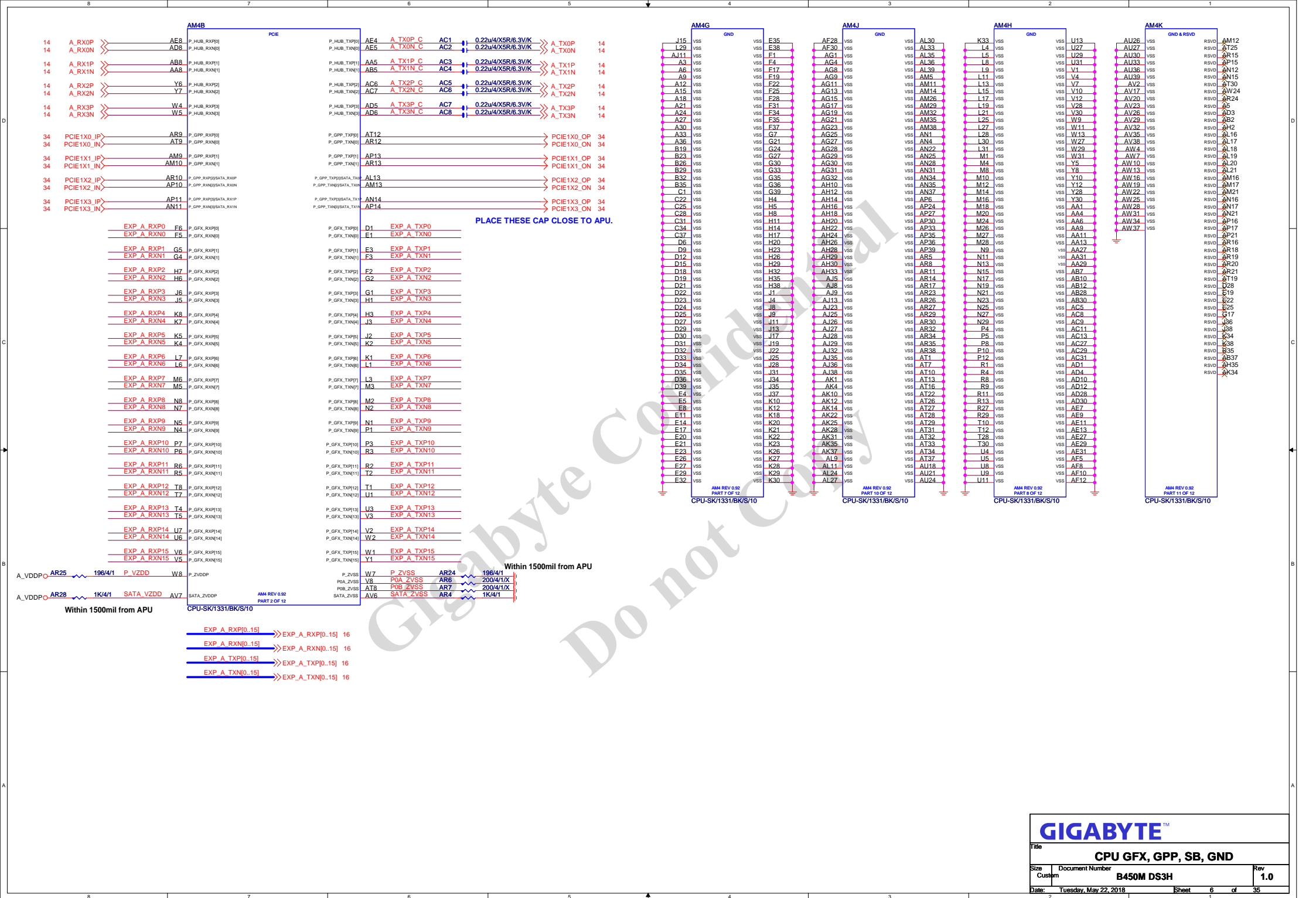
AM4 CPU CoreType			
CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0	1	Reserved	TYPE 1
1 ST	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

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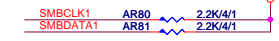
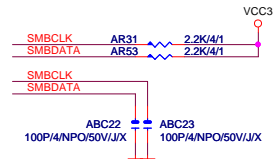
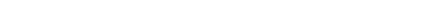
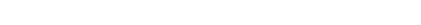
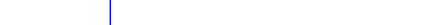
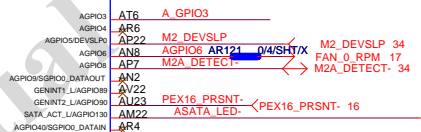
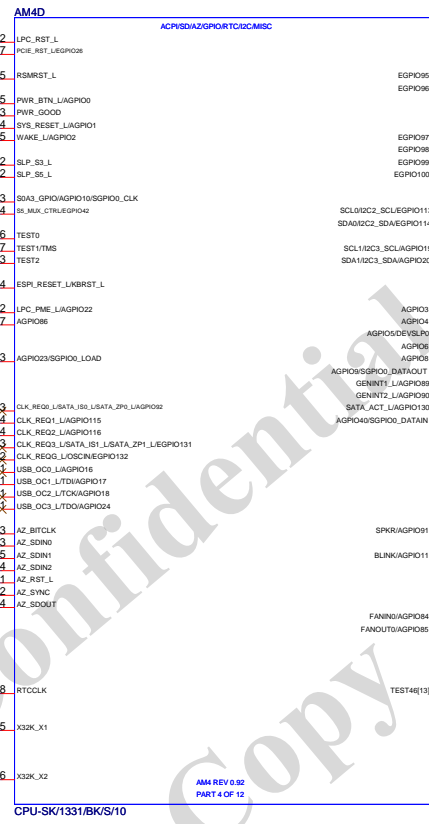
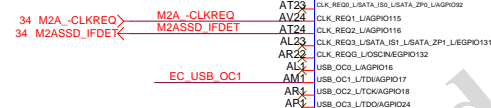
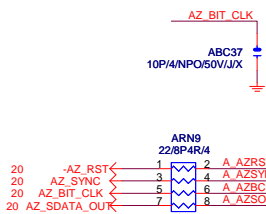
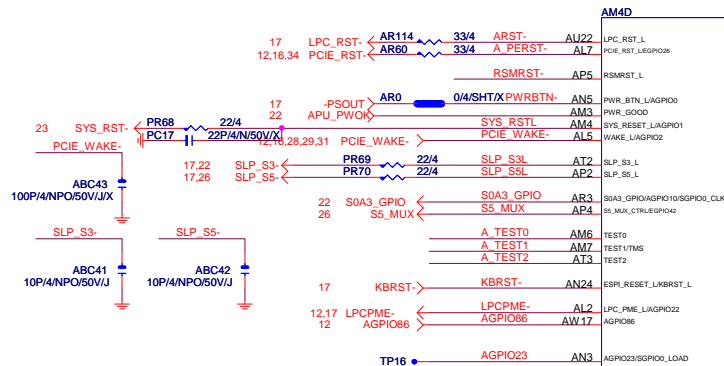
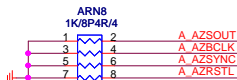
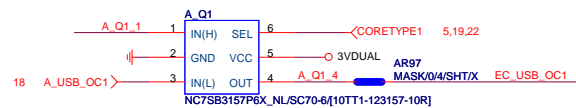
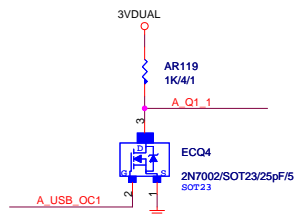
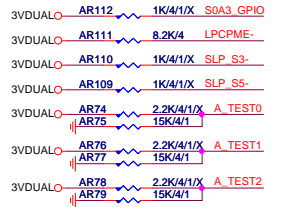
TitleCPU DDI, CONTROL

SizeCustomDocument NumberB450M DS3HRev1.0

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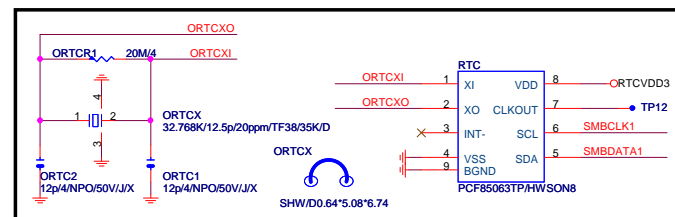


F. PANEL 已 PU



Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

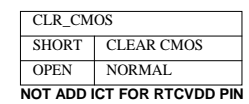
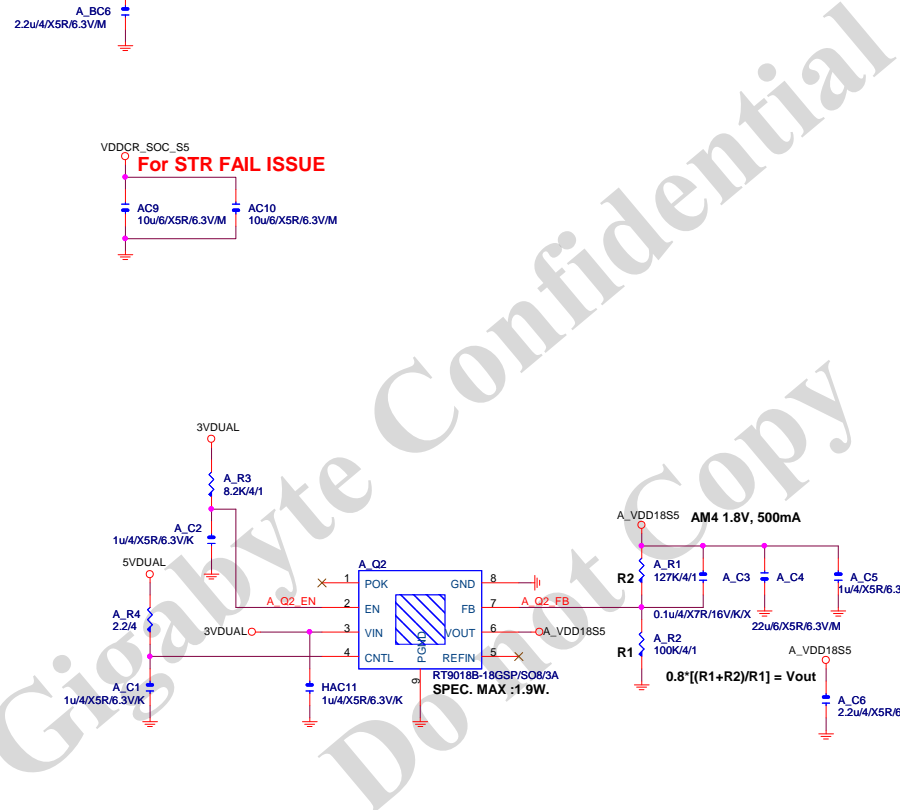


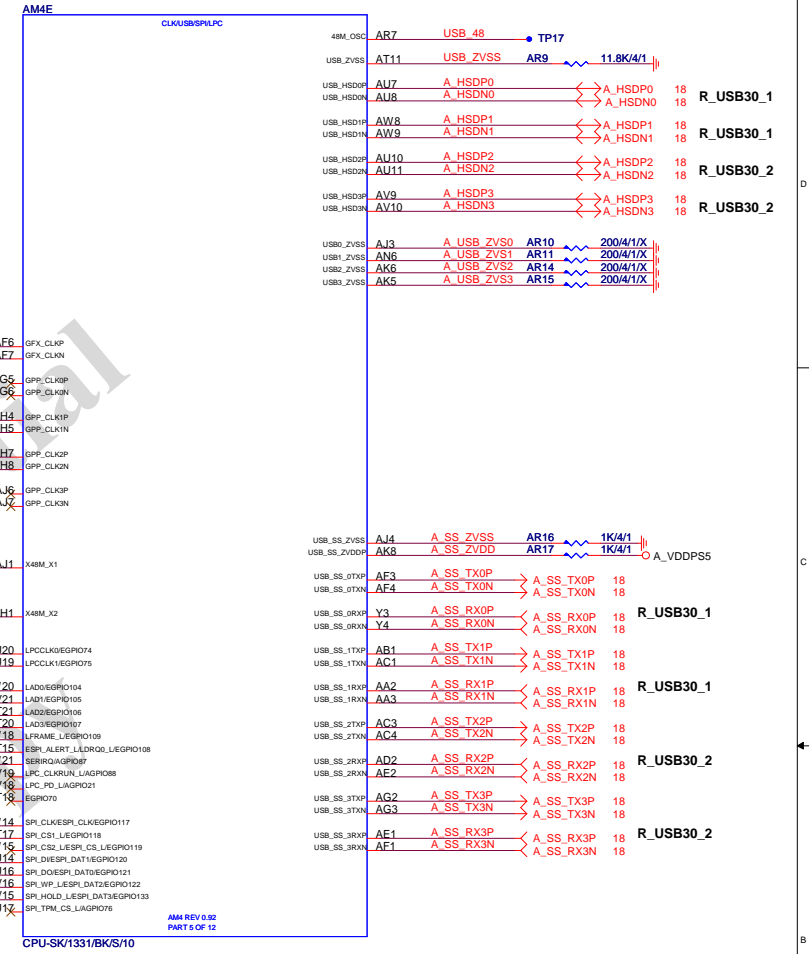
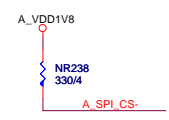
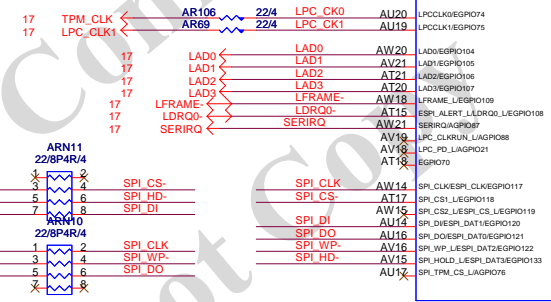
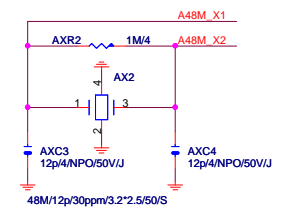
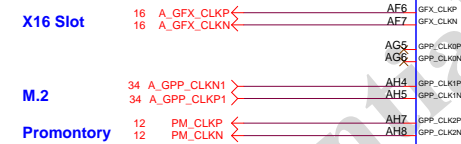
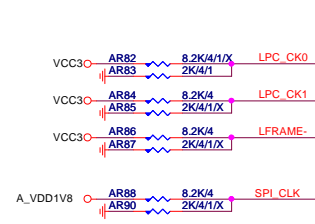
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Title AM4 MISC

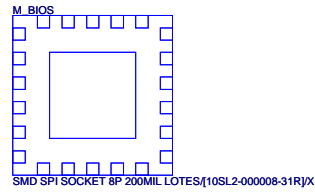
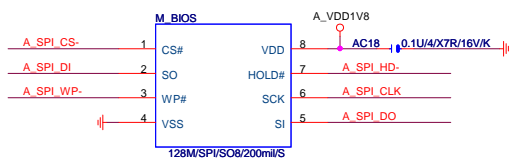
Size Custom Document Number B450M DS3H Rev 1.0

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128Mb: 128M/SPI/SO8/200mil/S
256Mb: 256M/WSON8/200MIL/S
Footprint: IC8WSON-BIOS-COLAY

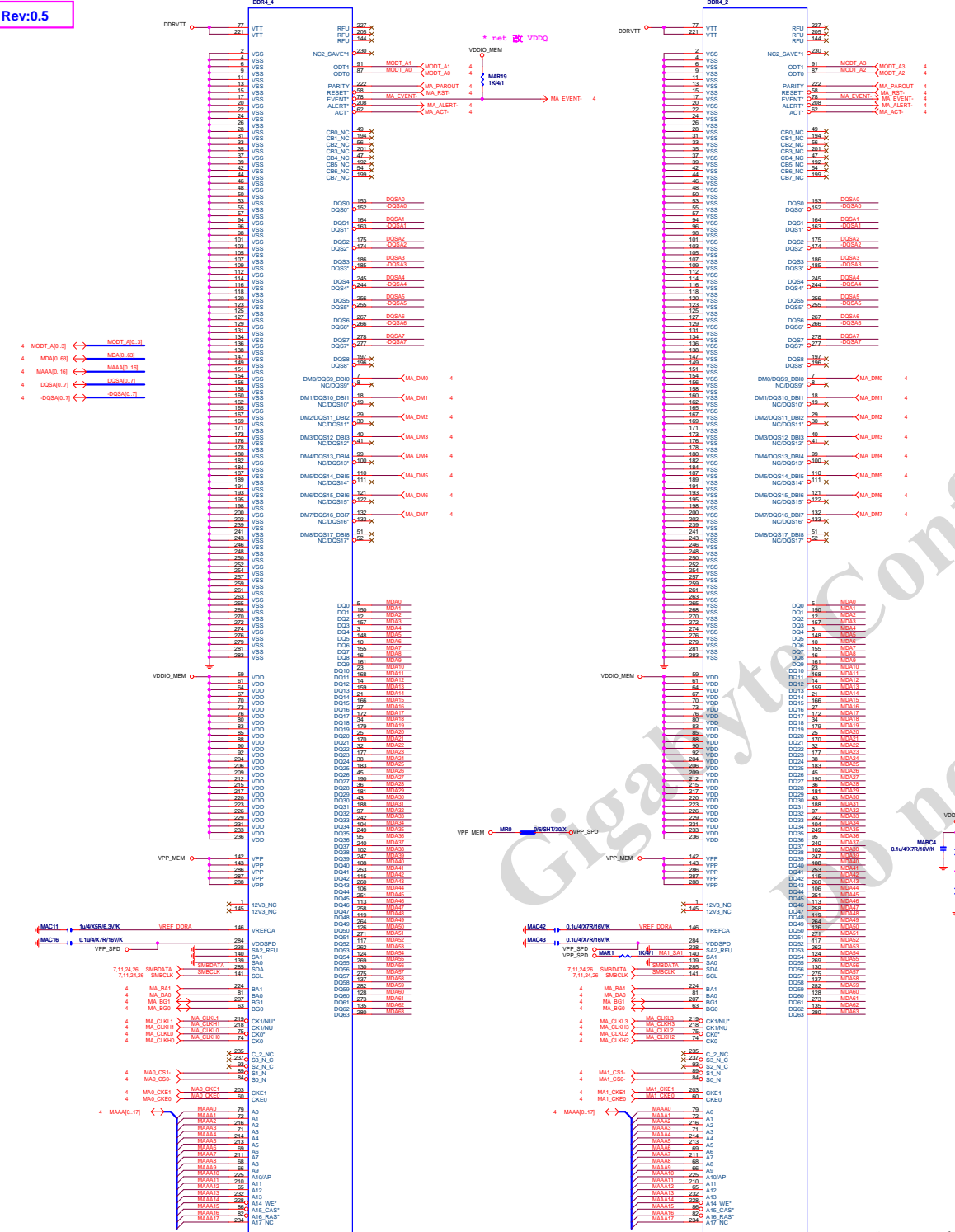


GIGABYTE™

TitleCPU USB3, SPI

SizeCustomDocument NumberB450M DS3HRev1.0

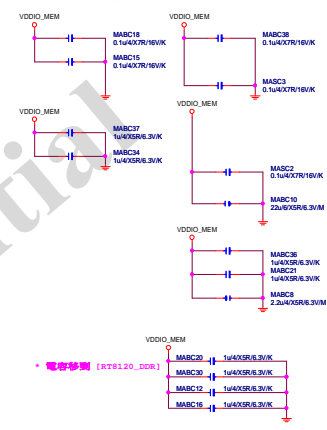
DateTuesday, May 22, 2018Sheet9 of 35



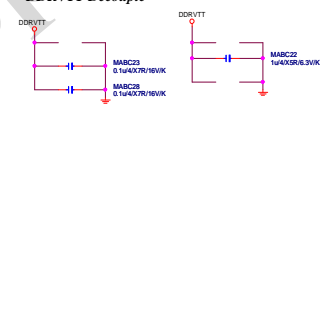
CHANNEL A0
SA2:0=000

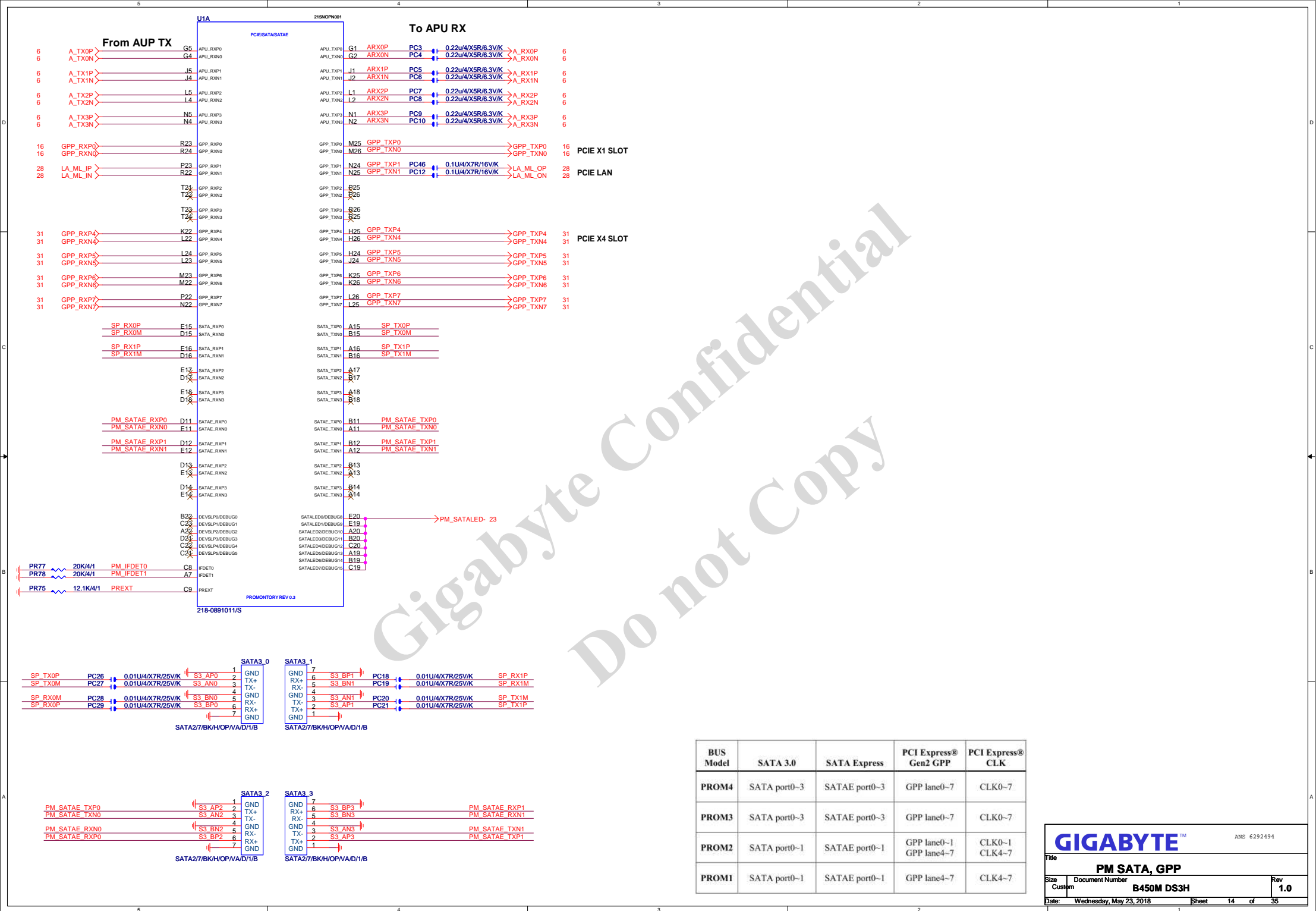
CHANNEL A1
SA2:2=010

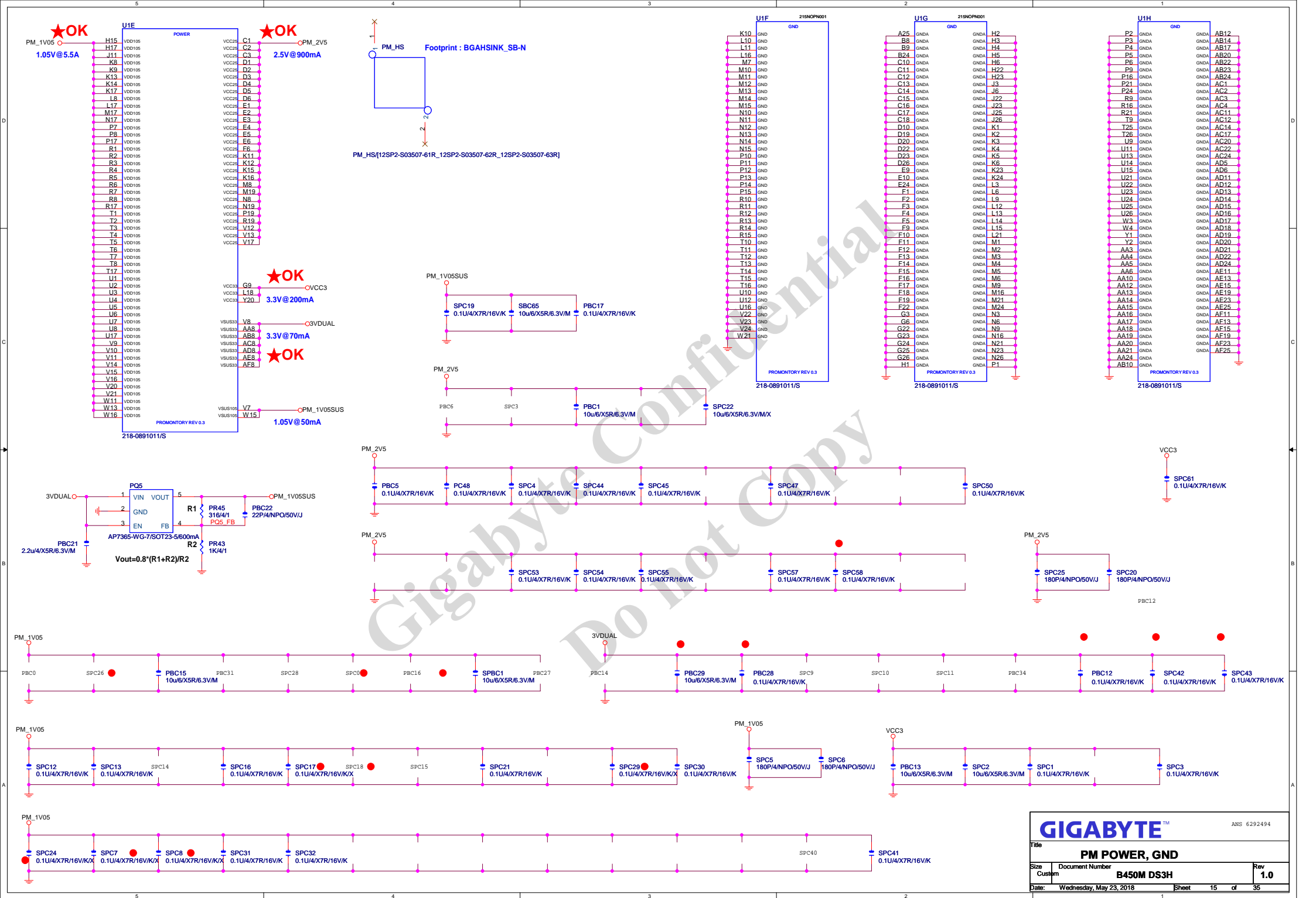
DDR12V Decouple

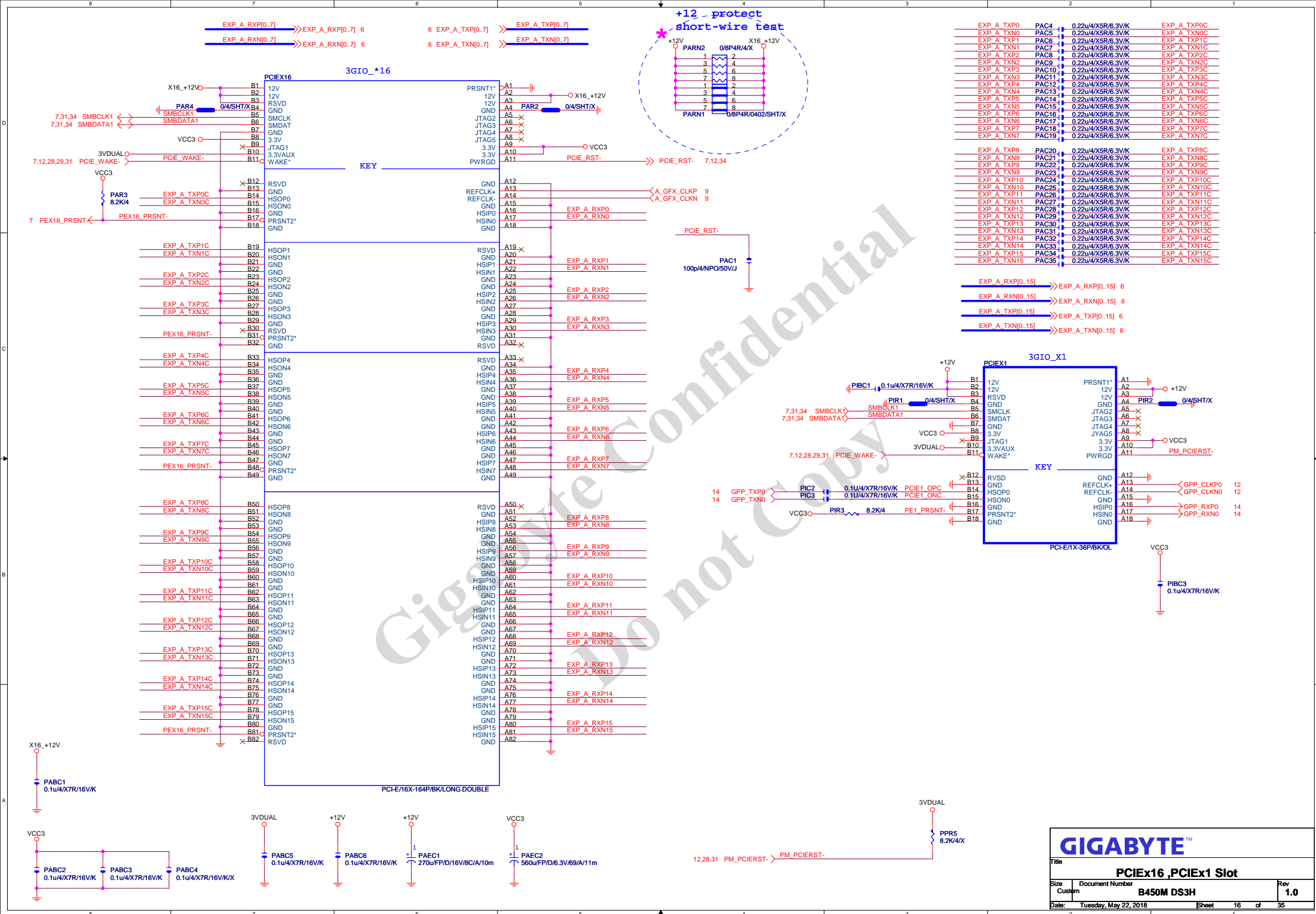


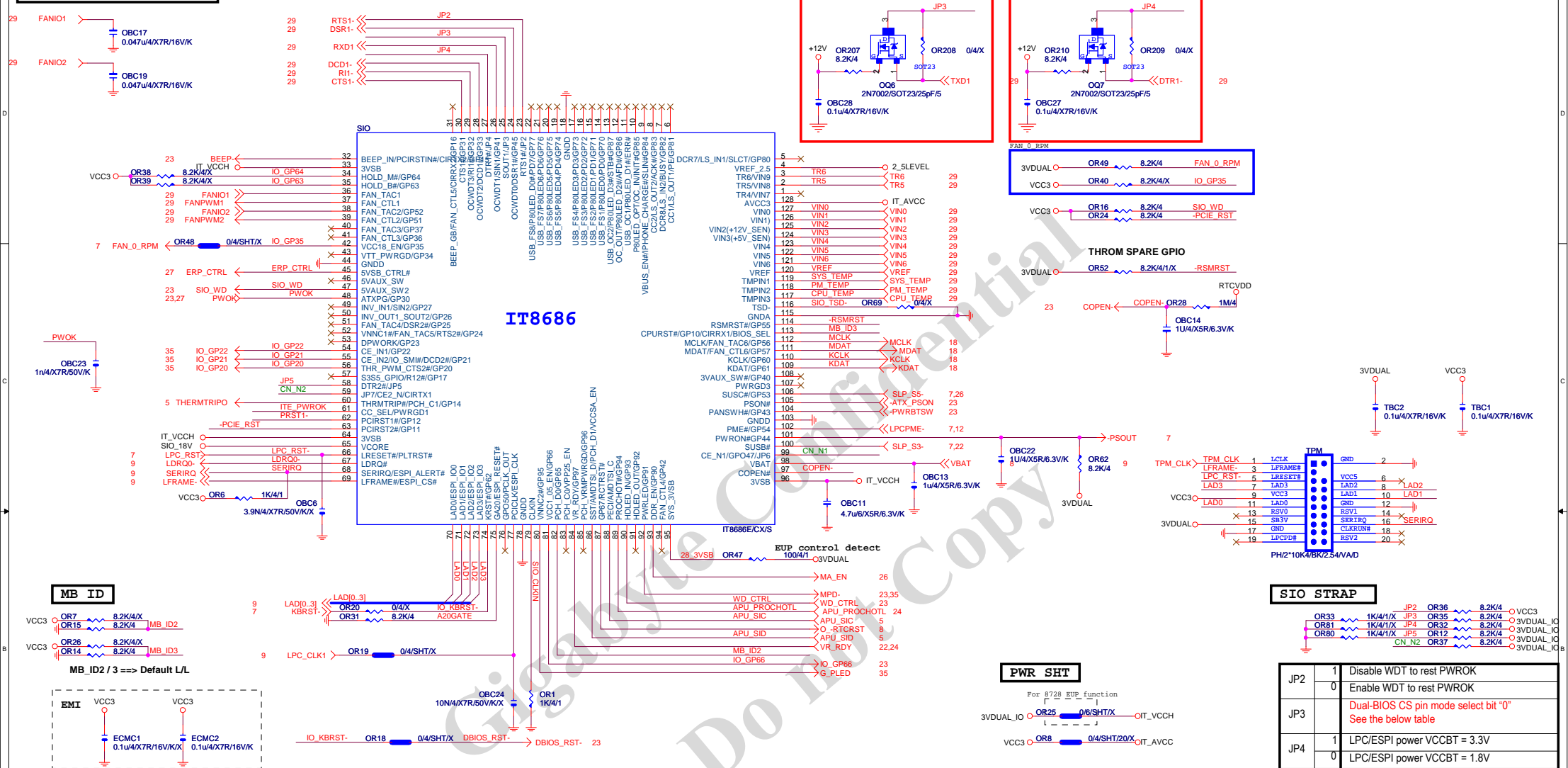
DDRVRTT Decouple





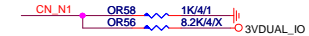




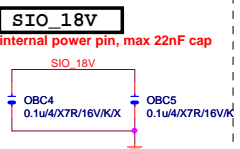


FAN TABLE		
	CPU_FAN	FAN_CTL1 FAN_TAC1
	SYS_FAN1	FAN_CTL2 FAN_TAC2
	SYS_FAN2	FAN_CTL3 FAN_TAC3
	SYS_FAN3	FAN_CTL4 FAN_TAC4
	OPT_FAN4 OR SYS_FAN4	FAN_CTL5 FAN_TAC5
	THRMTRIP	PIN56
	PROCHOT	PIN89

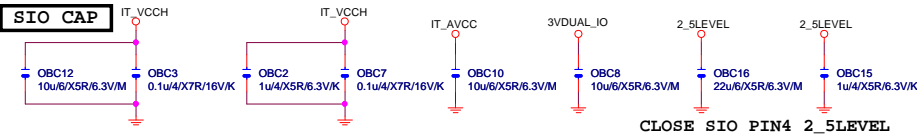
DUAL BIOS OPT STRAP



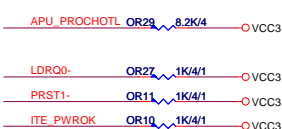
Power leakage



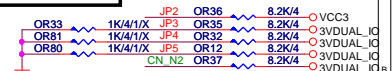
SIO CAP



SIO PU



SIO STRAP

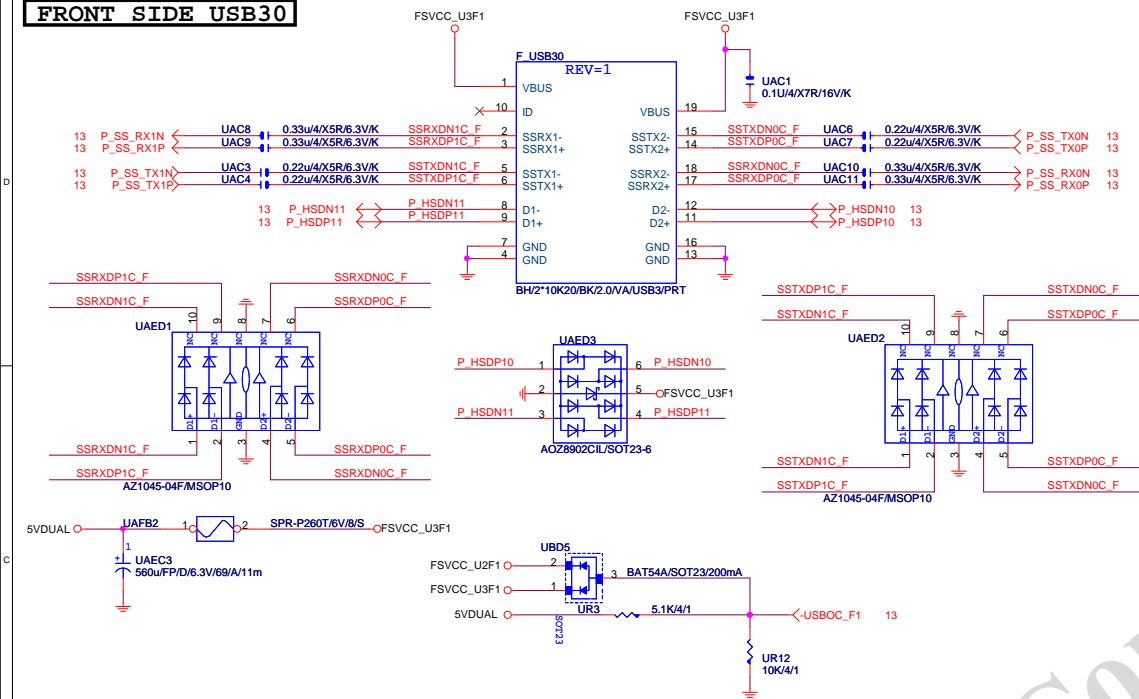


JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

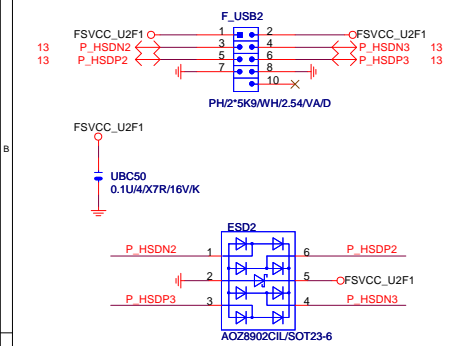
GIGABYTE™

Title			
ITE 8686 LPC IO			
Size	Document Number	Rev	
Custom	B450M DS3H	1.0	
Date:	Tuesday, May 22, 2018	Sheet	17 of 35

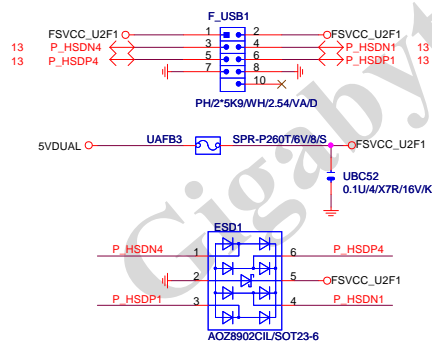
FRONT SIDE USB30



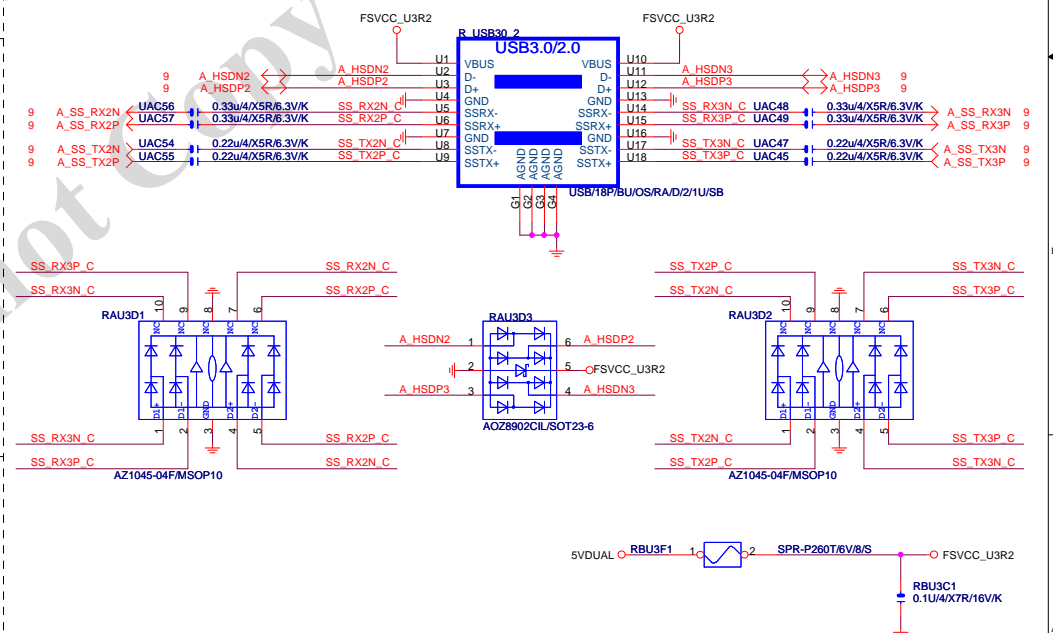
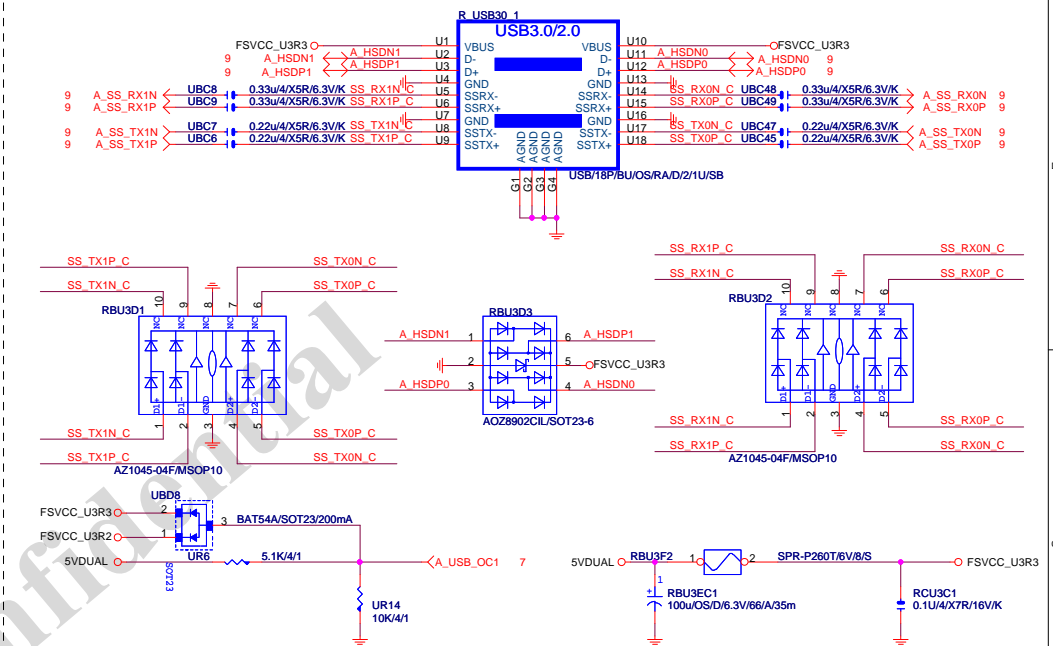
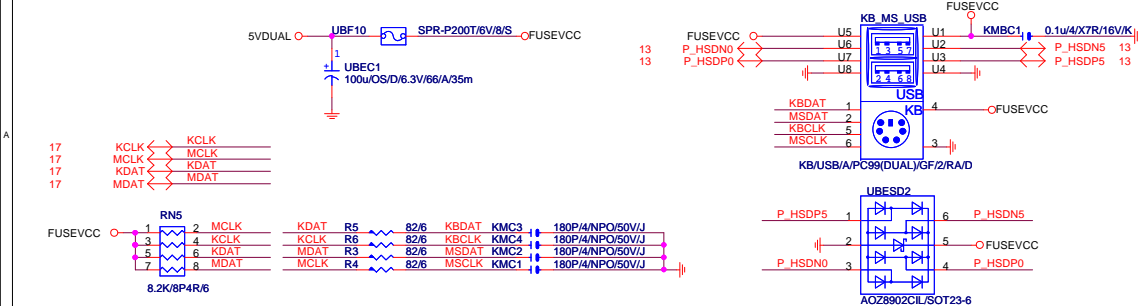
FRONT SIDE USB2



FRONT SIDE USB1



KB/MS & USB

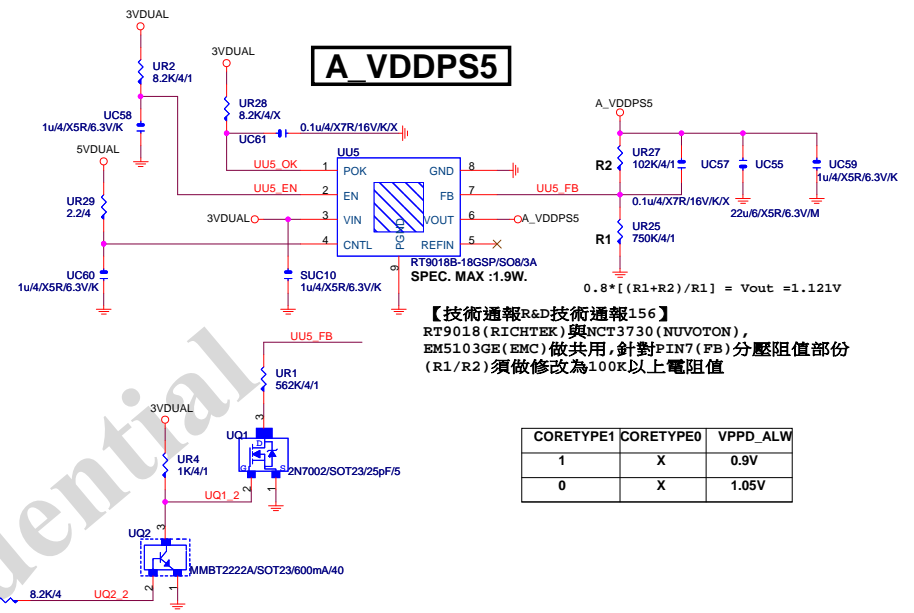


GIGABYTE™

Title	F_USB ,F_USB30 ,R_USB30 , KB_MS_USB
-------	-------------------------------------

Size Custom	Document Number B450M DS3H	Rev 1.0
Date: Tuesday, May 22, 2018	Sheet 18 of 35	

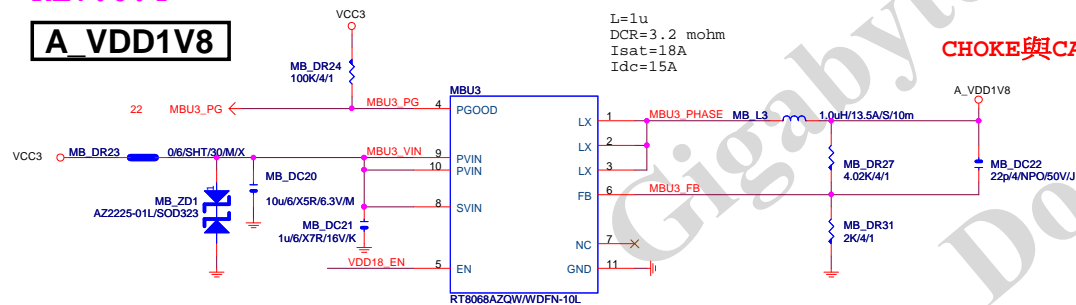
A_VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

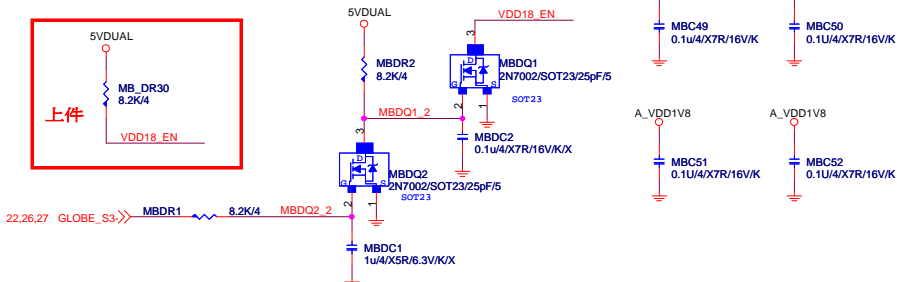
REV:0.4

A_VDD1V8



CHOKES與CAP料號可變

PWR SEQ

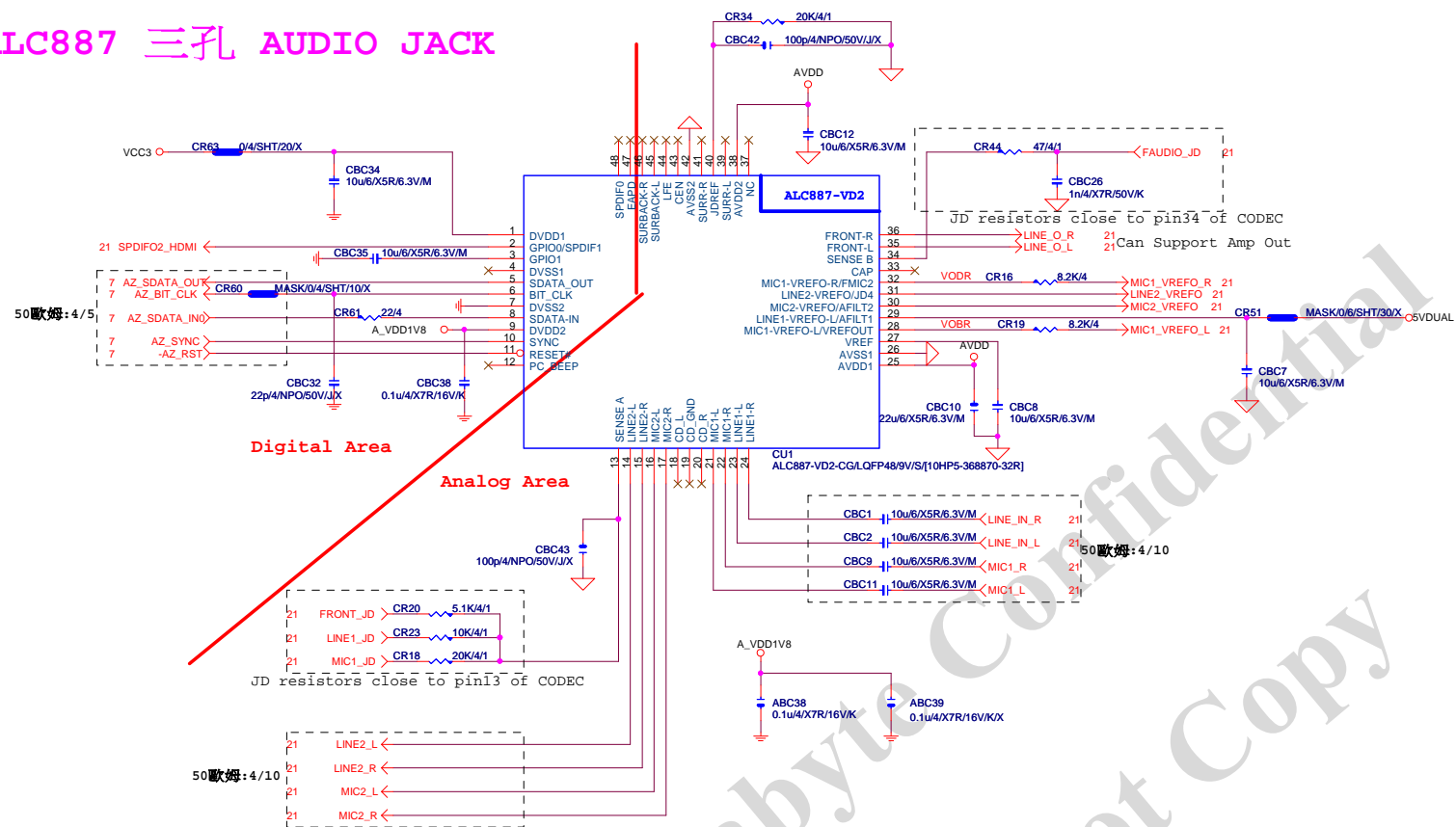


VPP CAP

★ 大電容 x0

 22u*1PCS

ALC887 三孔 AUDIO JACK



LAYOUT注意:螺絲孔下GND方式

- MH1空間夠,下DGND
空間不夠,改為Isolate
- MH2一律改為Isolate

<input type="radio"/> MH1	<input type="radio"/> MH2
DGND	Isolate

LAYOUT注意:要加

GND切割線

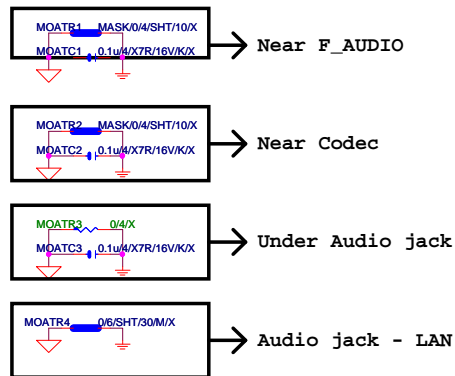
音效區域印刷



BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (上件與否,依照各Model spec)
3. LED Reserve (上件與否和LED顏色,依照各Model spec)

GIGABYTE™			
Title ALC887 CODEC			
Size	Document Number	Rev	
Custom	B450M DS3H	1.0	
Date:	Tuesday, May 22, 2018	Sheet	20 of 35

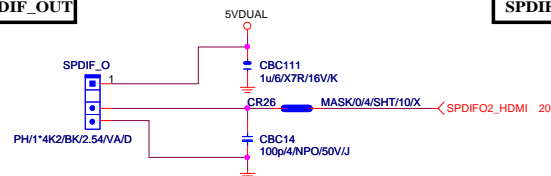
Rev 3.1



*量産前,0ohm改short pad

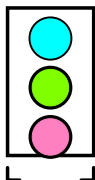
SPDIF_OUT

SPDIF_IN

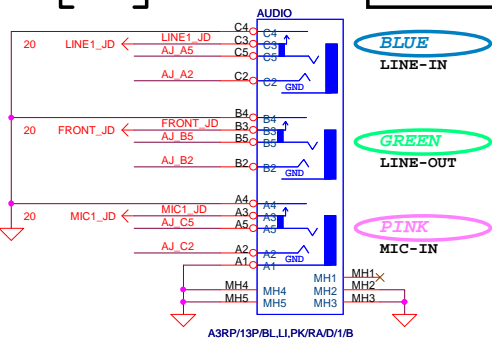


For HDMI SPDIF (依SPEC保留或移除)

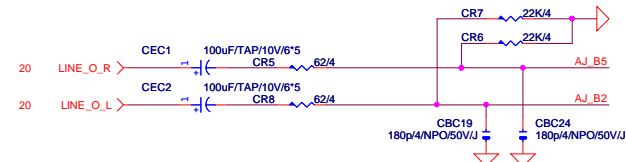
AZALIA JACK



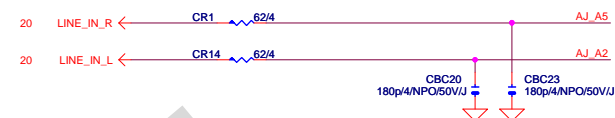
AZALIA JACK



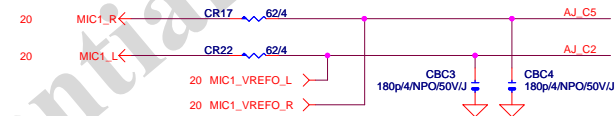
LINE-OUT



LINE-IN



MIC-IN

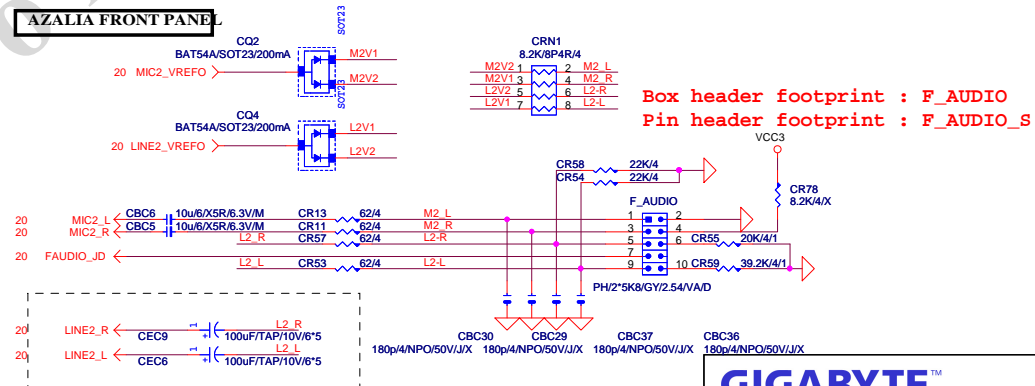


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL



GIGABYTE™

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	B450M DS3H	1.0
Date:	Tuesday, May 22, 2018	Sheet 21 of 35

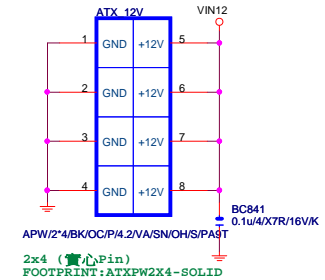
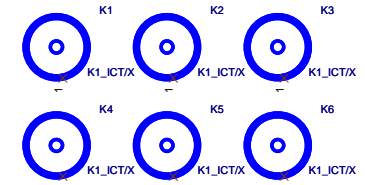
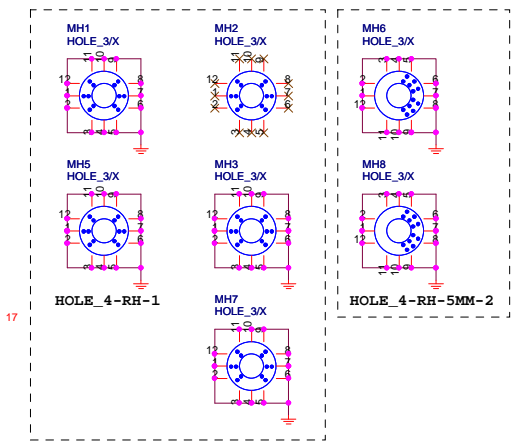
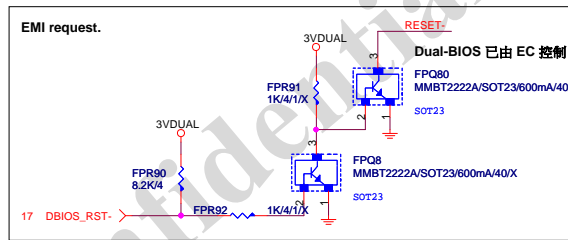
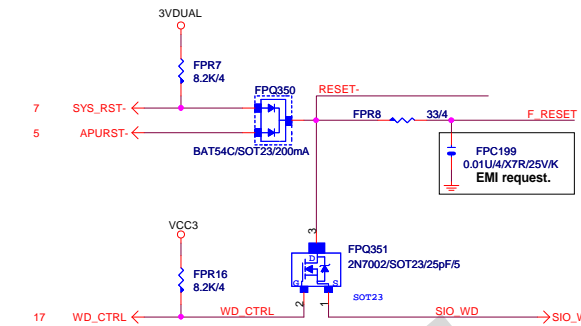
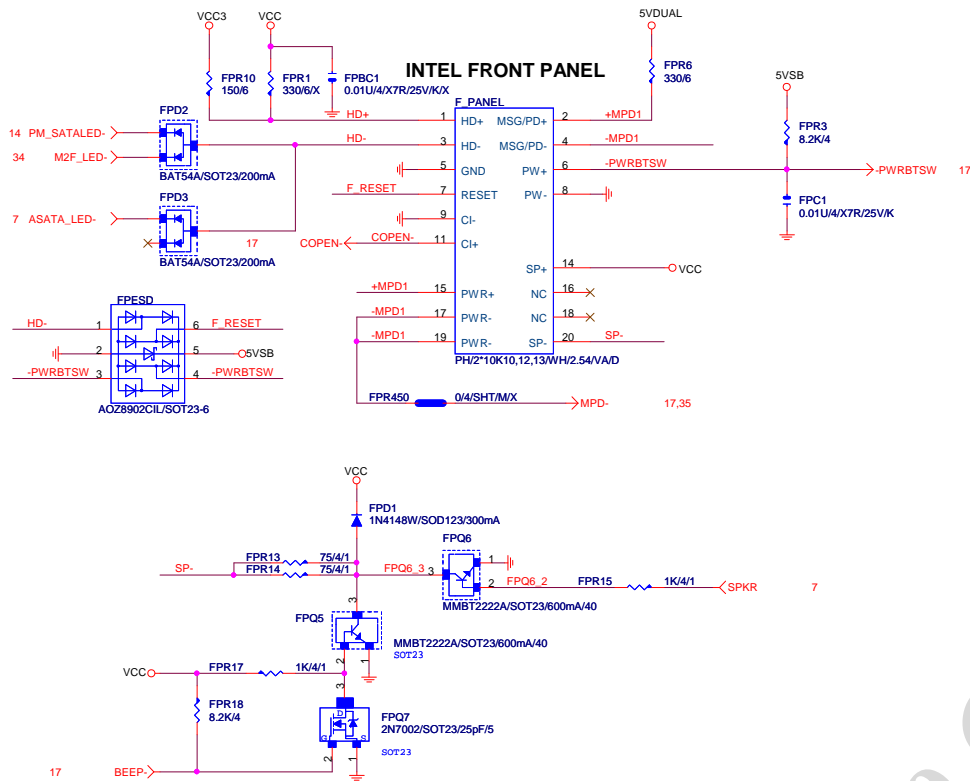


19 MBU3_PG) NPR18 0/4/SH17X AVDDP_EN



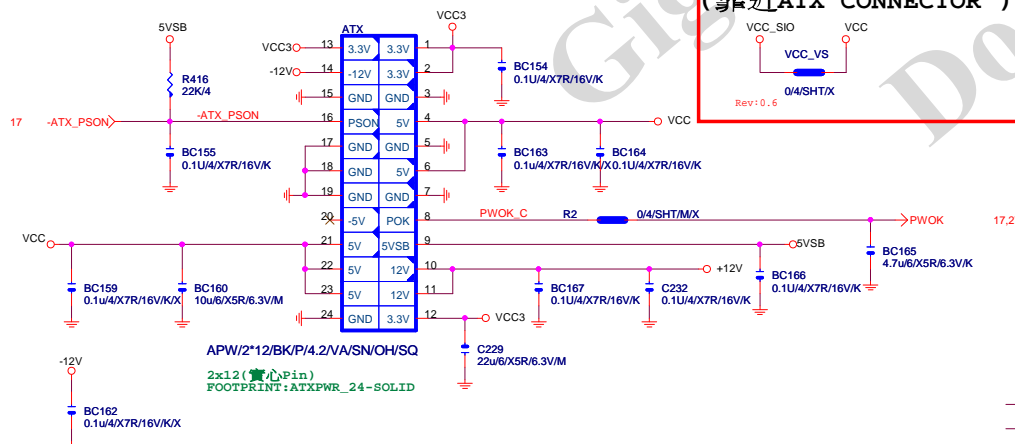
5,7,19 CORETYPE1 > CORETYPE1 PR85

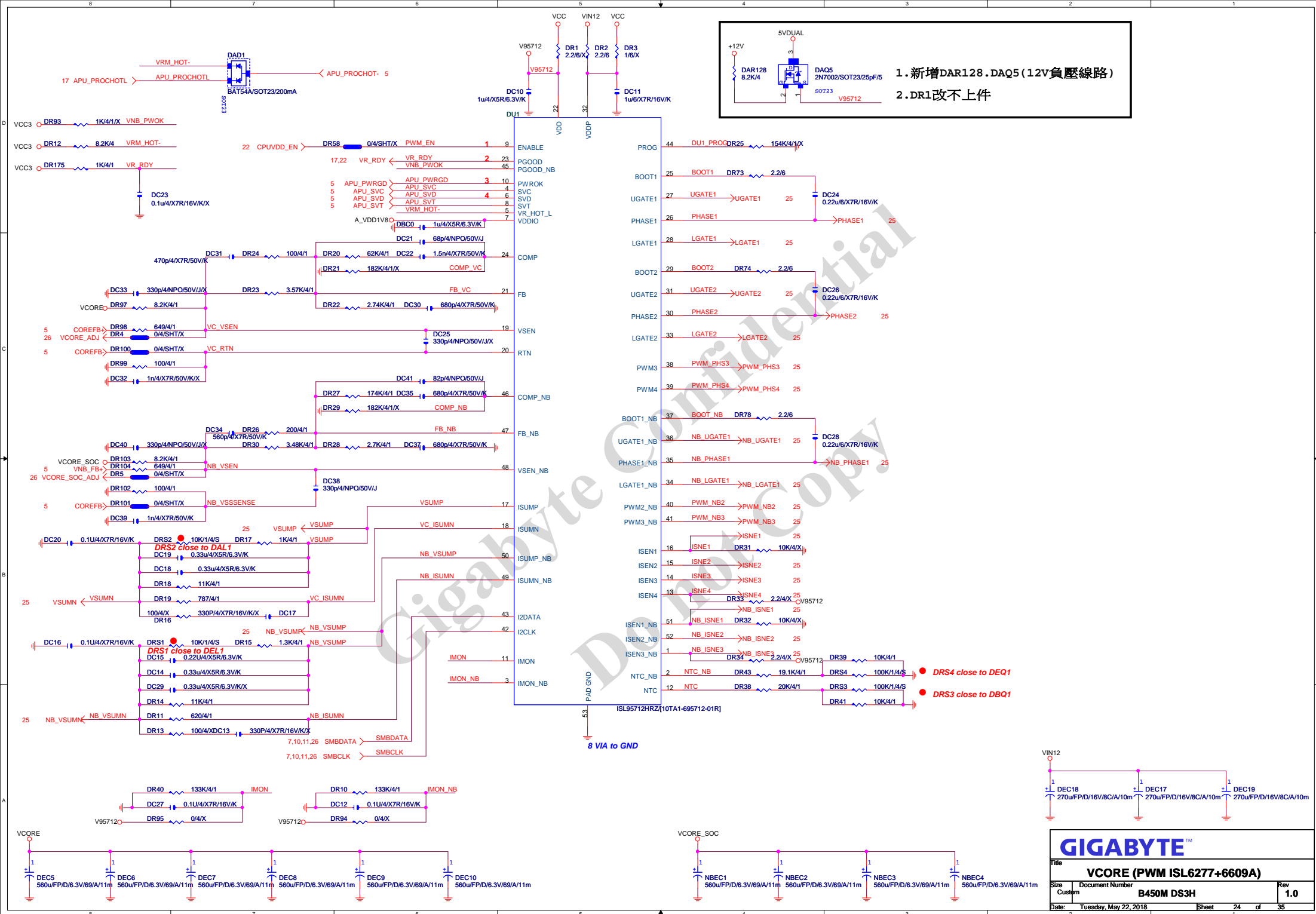


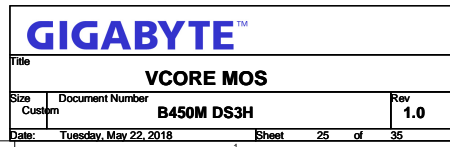


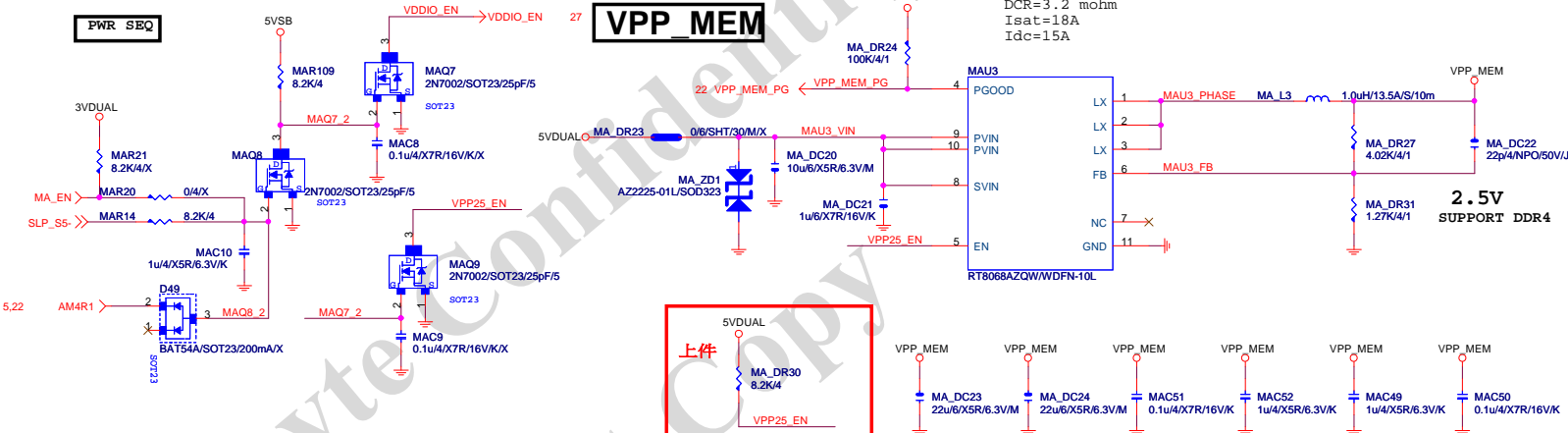
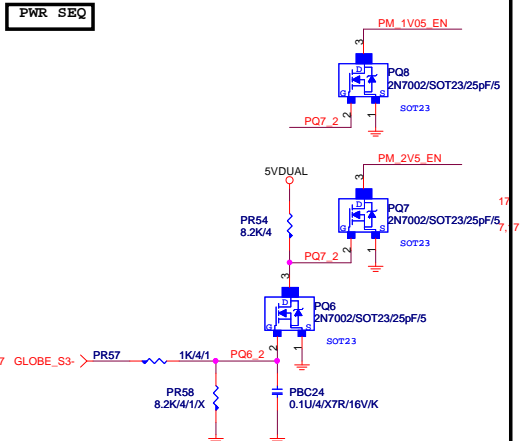
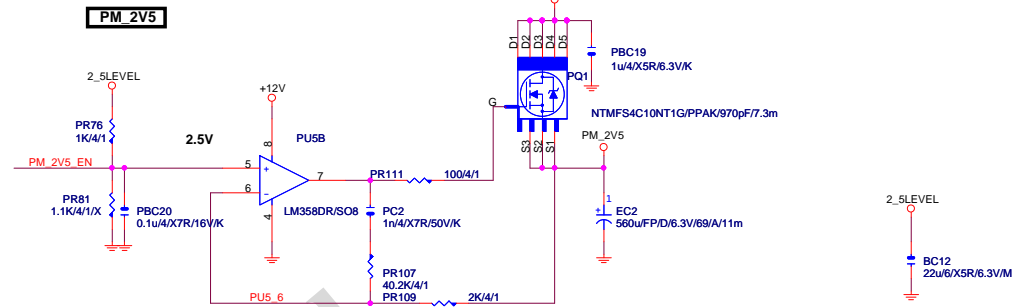
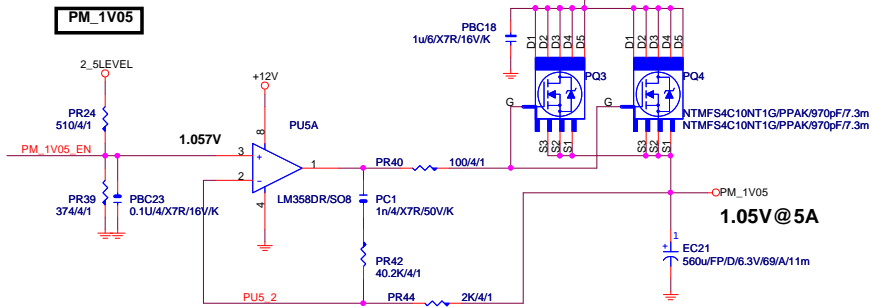
ATX POWER CONNECTOR

(靠近ATX CONNECTOR)

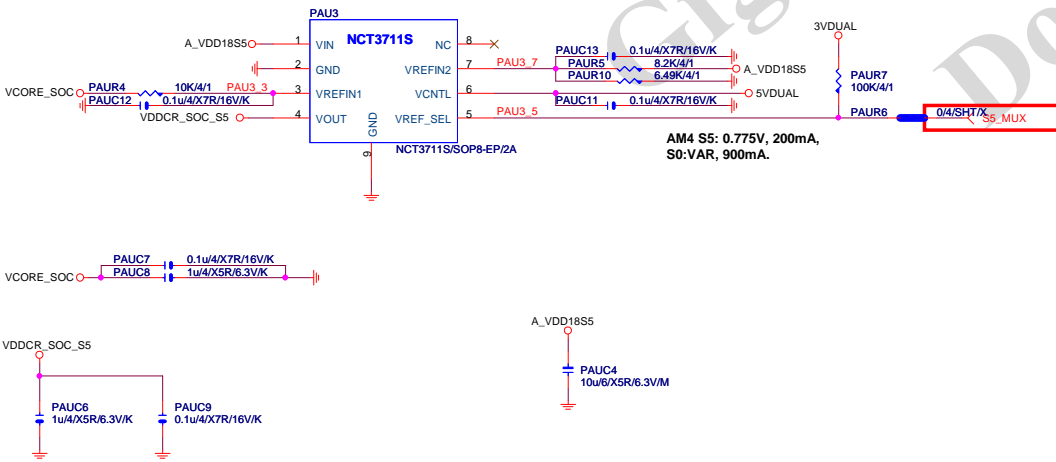




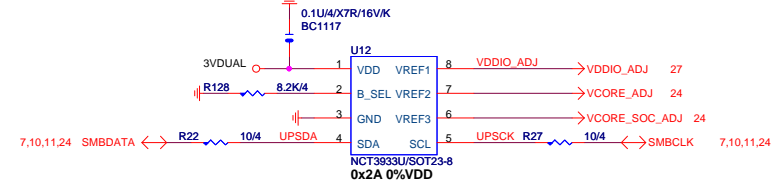




VDDCR SOC S5

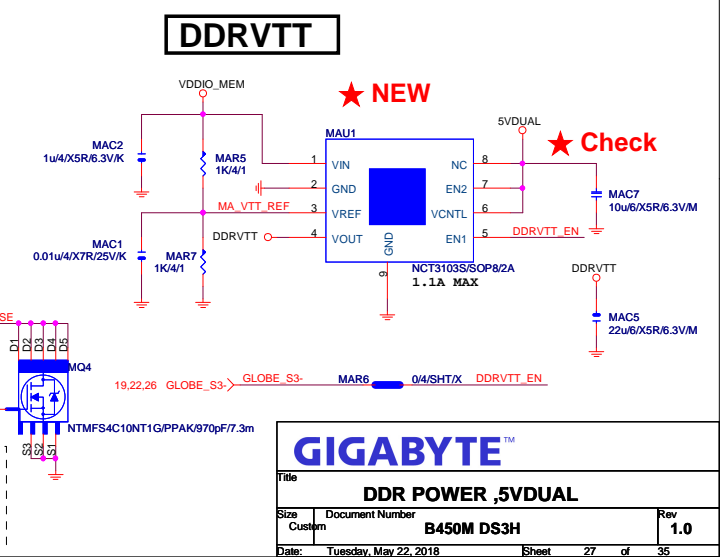
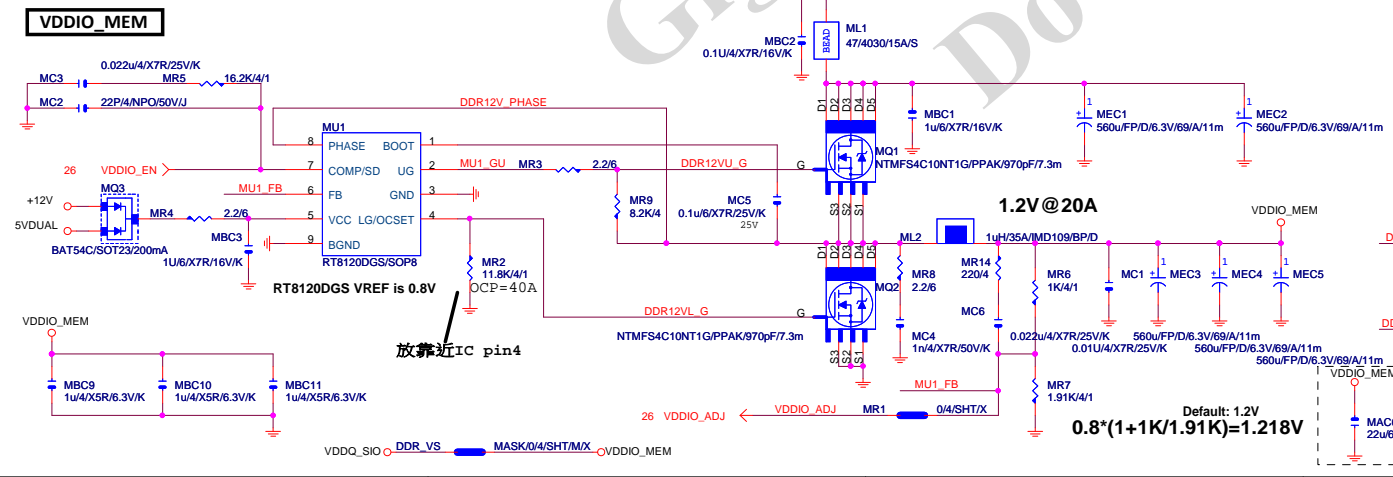
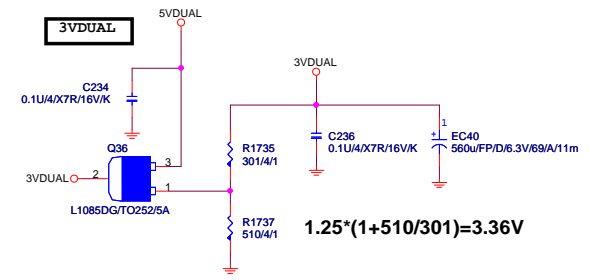
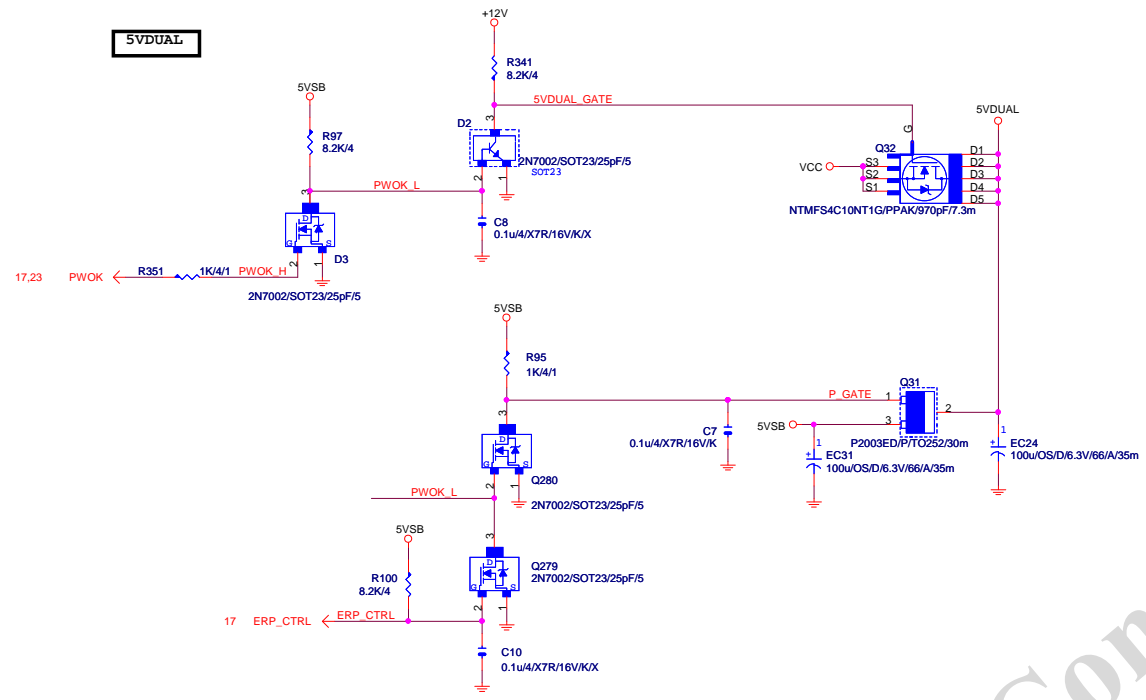


S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.



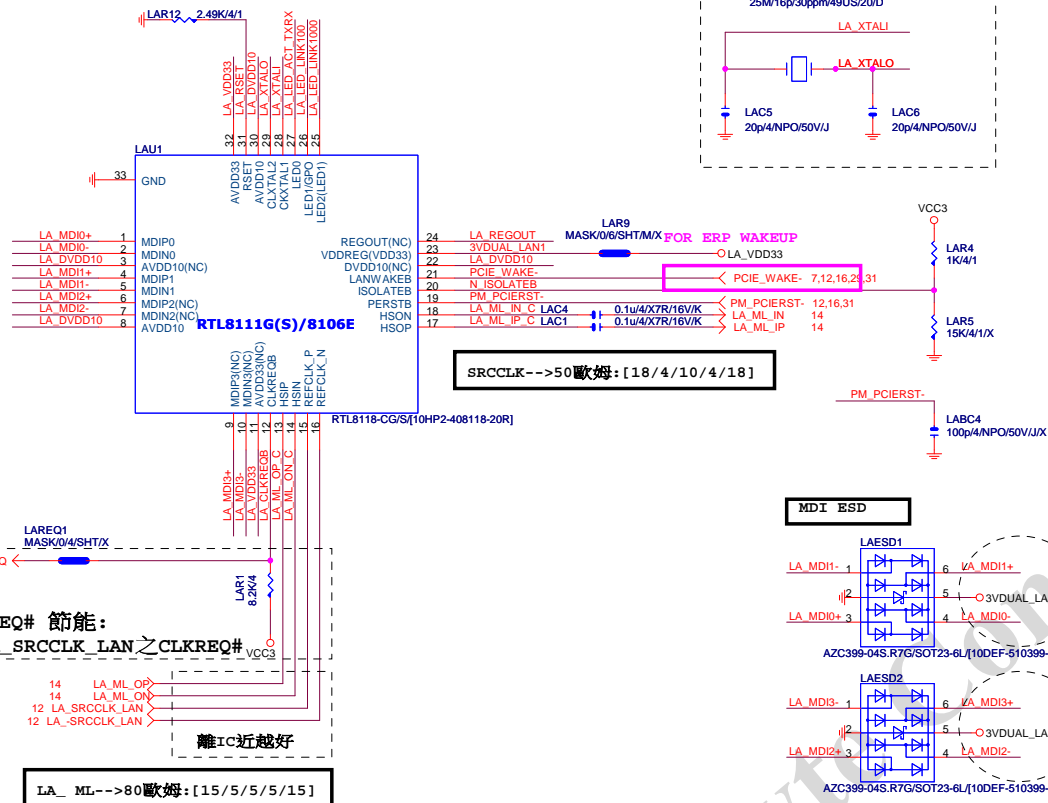
GIGABYTE

Title			
PM PWR,VPP_MEM,VDDCR_SOC_S5			
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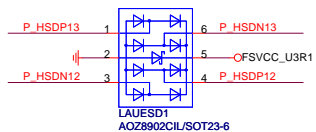
GIGABYTE™		
Title: DDR POWER ,5VDUAL		
Size: Custom	Document Number: B450M DS3H	Rev: 1.0
Date: Tuesday, May 22, 2018	Sheet: 27	of 35

LAN:RTL8118	R2.03
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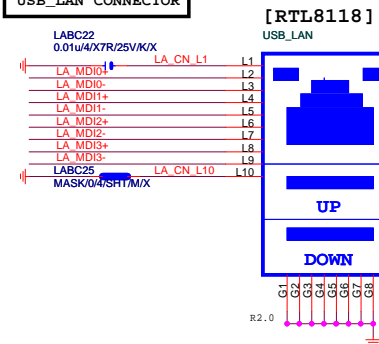


USB_LAN CONNECTOR	R2.03
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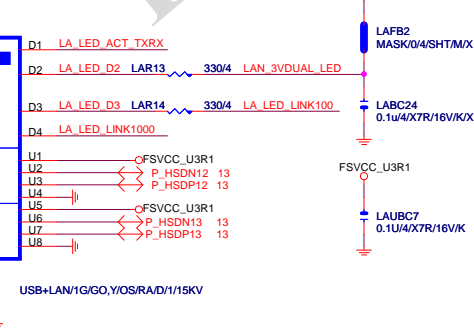
RMA ESD PROTECT



USB_LAN CONNECTOR

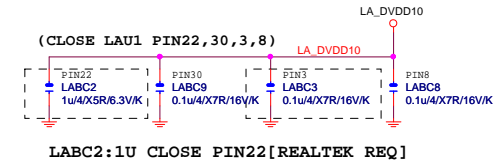


[RTL8118]



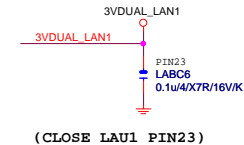
LA_MDI-->100歐姆:[20/4/8/4/20]

LAN POWER

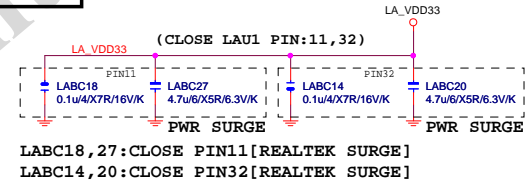


LAN POWER

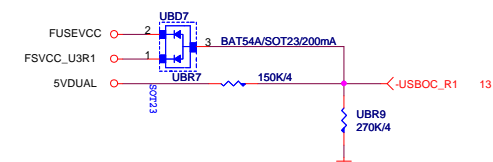
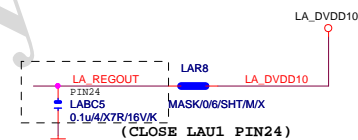
note: lan power連接及電流



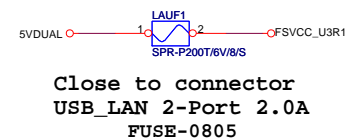
LAN POWER



LAN POWER



USB POWER



LAN POWER

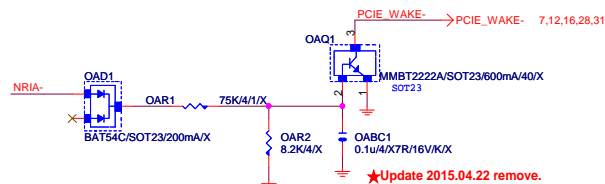
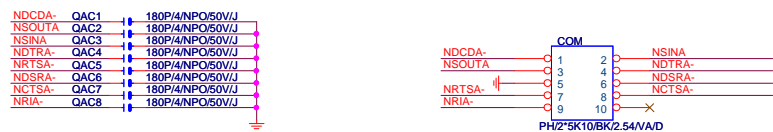
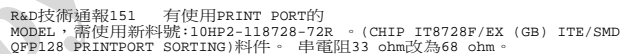


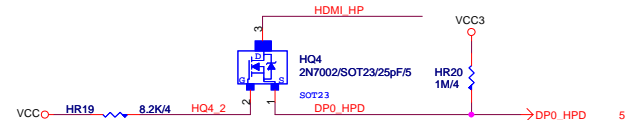
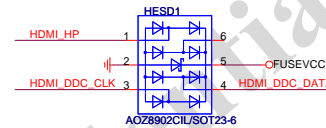
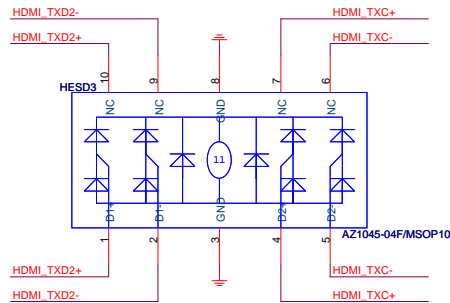
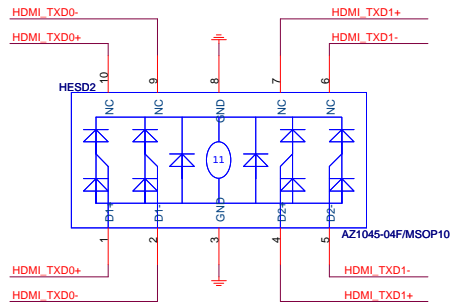
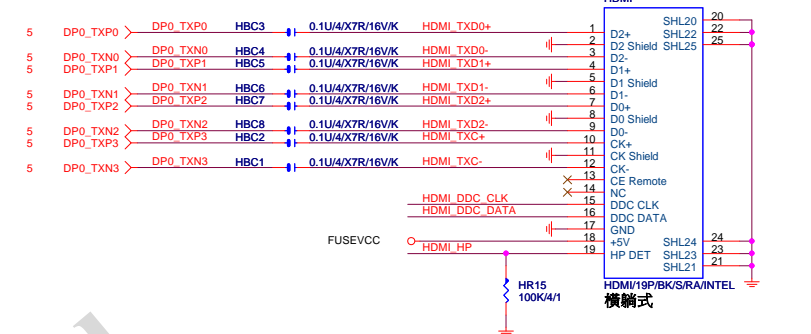
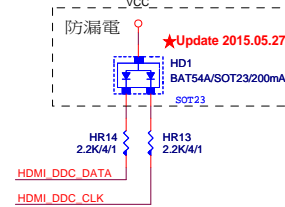
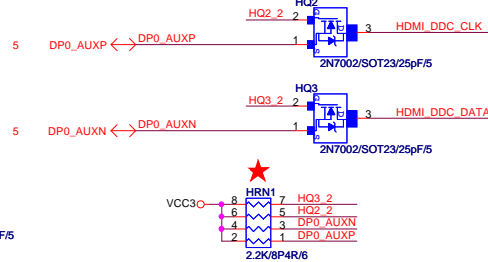
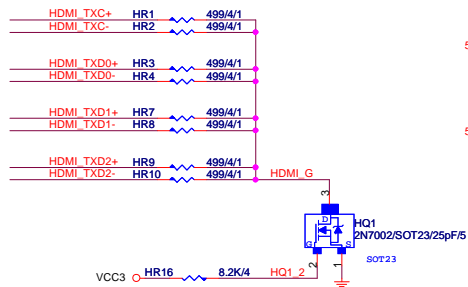
EMI

LAN AGND change GND
Remove Short Pad

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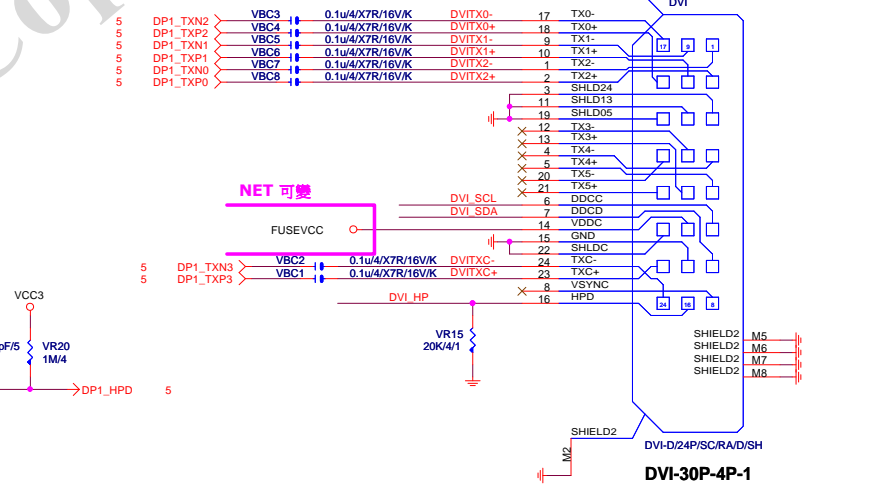
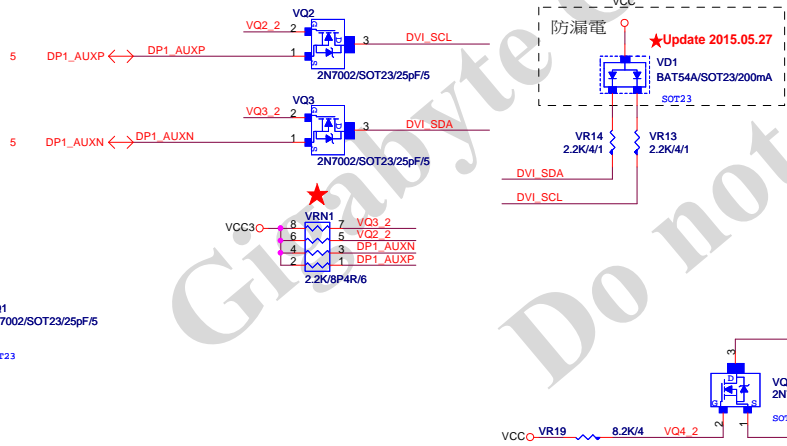
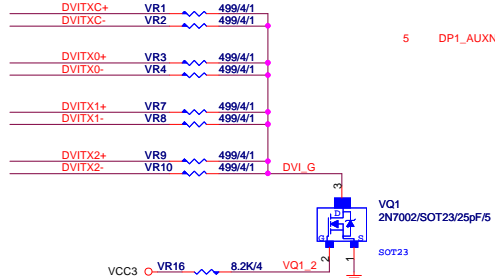




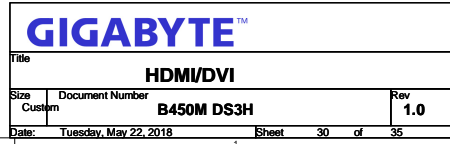
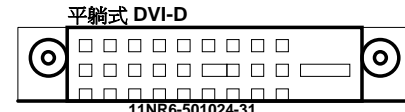
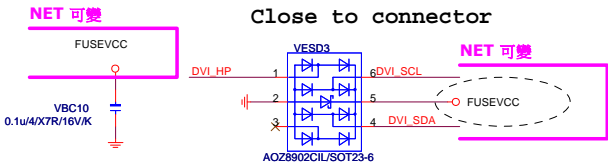
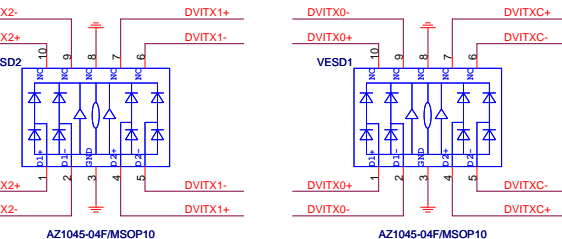
Rev: 0.73

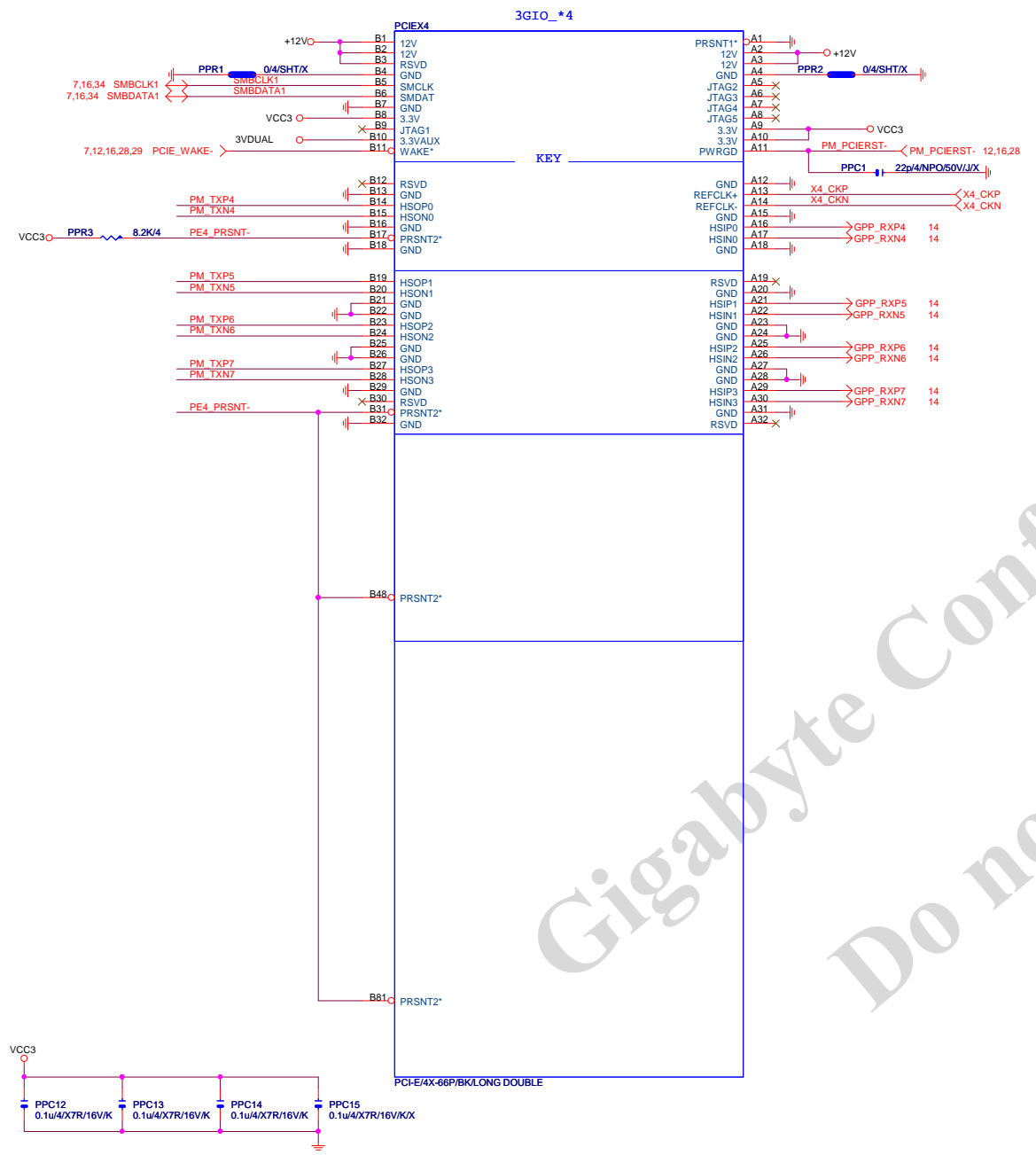
DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%

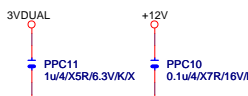


Close to connector



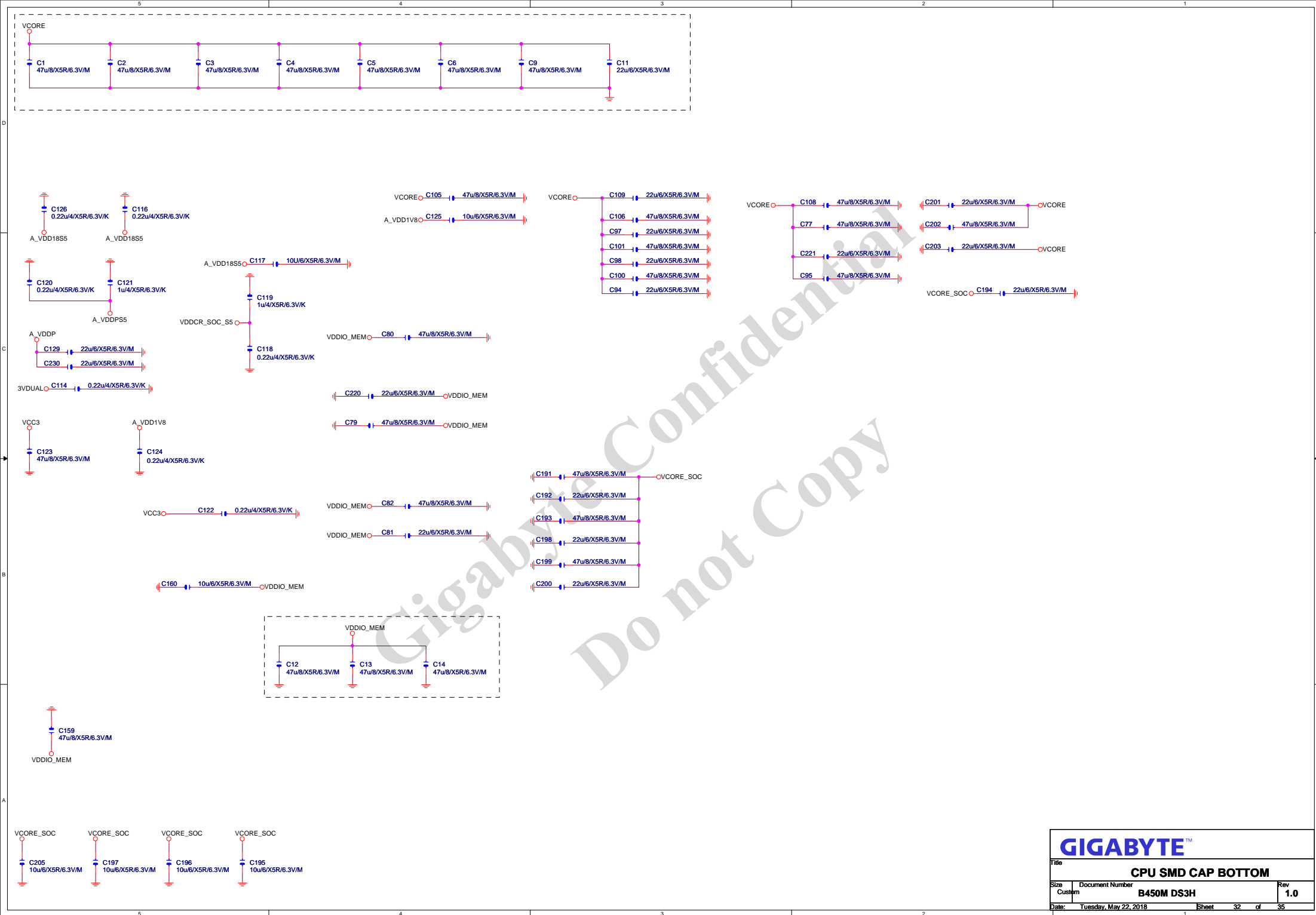


14	GPP_TXP4	GPP_TXP4	PPC2	0.1u/4/X7R/16V/K	PM_TXP4
14	GPP_TXN4	GPP_TXN4	PPC3	0.1u/4/X7R/16V/K	PM_TXN4
14	GPP_TXP5	GPP_TXP5	PPC4	0.1u/4/X7R/16V/K	PM_TXP5
14	GPP_TXN5	GPP_TXN5	PPC5	0.1u/4/X7R/16V/K	PM_TXN5
14	GPP_TXP6	GPP_TXP6	PPC6	0.1u/4/X7R/16V/K	PM_TXP6
14	GPP_TXN6	GPP_TXN6	PPC7	0.1u/4/X7R/16V/K	PM_TXN6
14	GPP_TXP7	GPP_TXP7	PPC8	0.1u/4/X7R/16V/K	PM_TXP7
14	GPP_TXN7	GPP_TXN7	PPC9	0.1u/4/X7R/16V/K	PM_TXN7

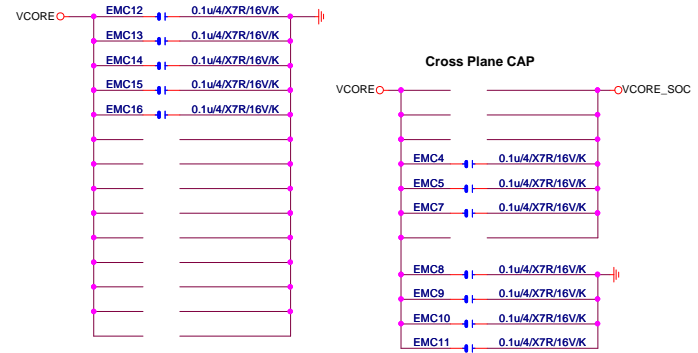


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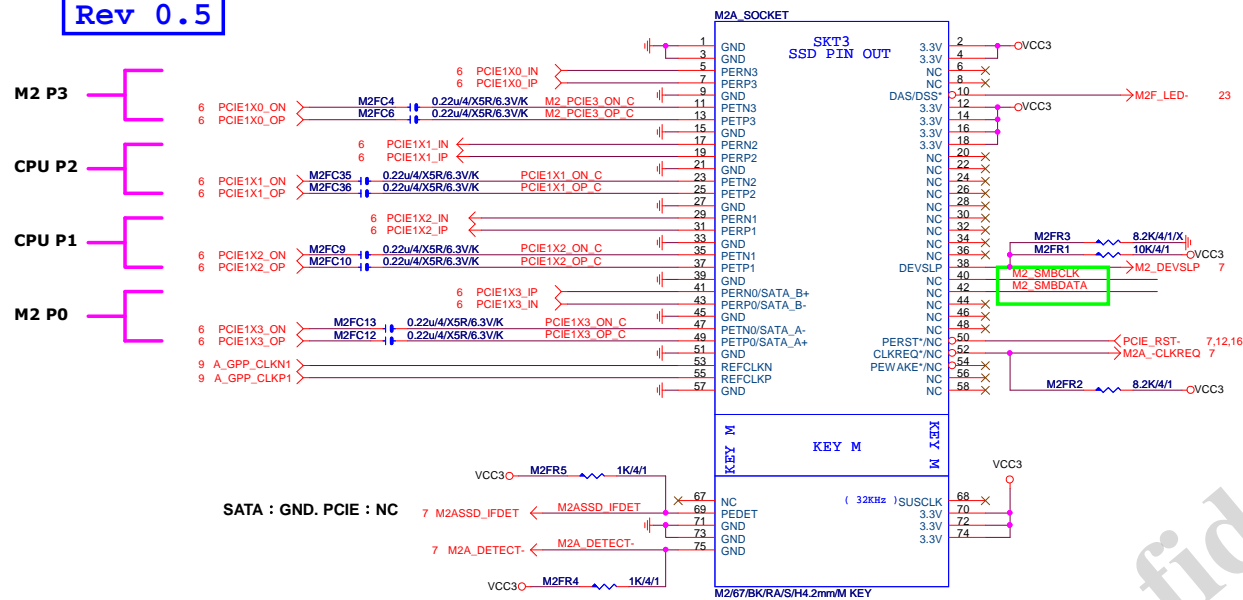
Title		
PCIe4 Slot		
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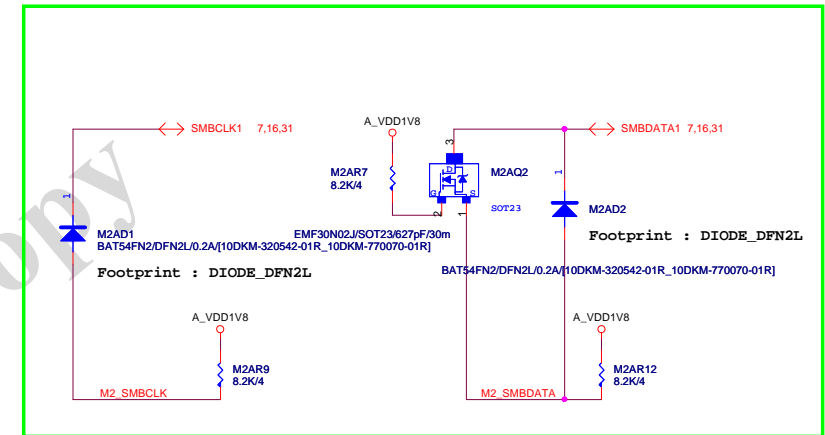
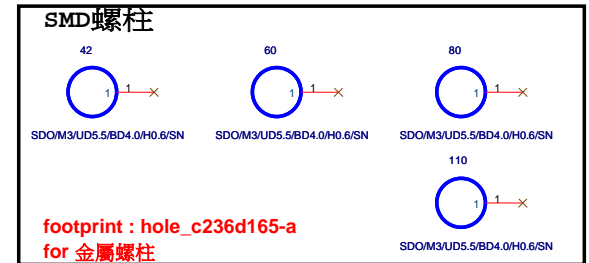
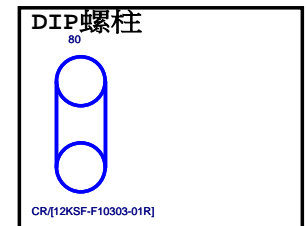
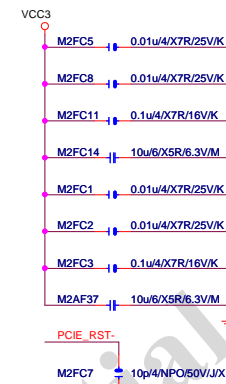
CPU TOP CAVITY

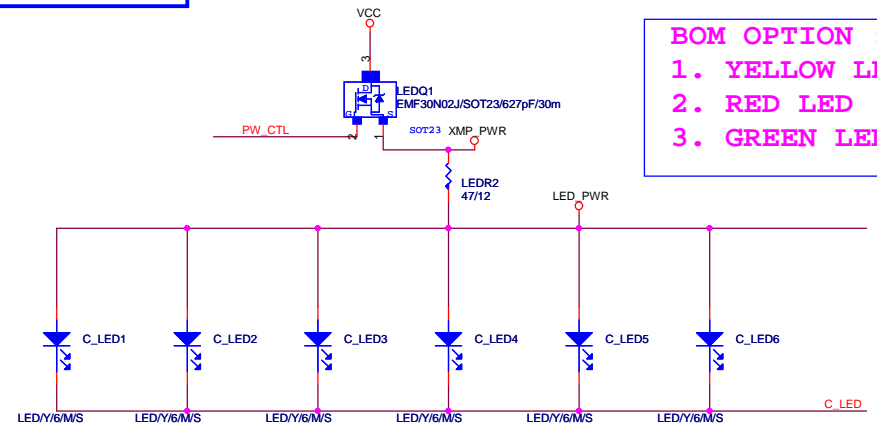


Rev 0.5

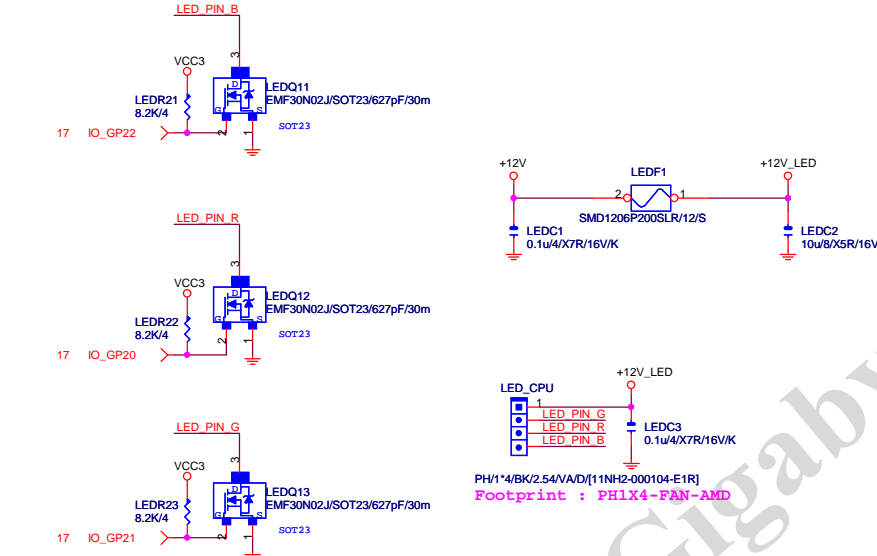


footprint : NGFF-M-75P-11CM-09MM-SMD





RGB LED CONTROL



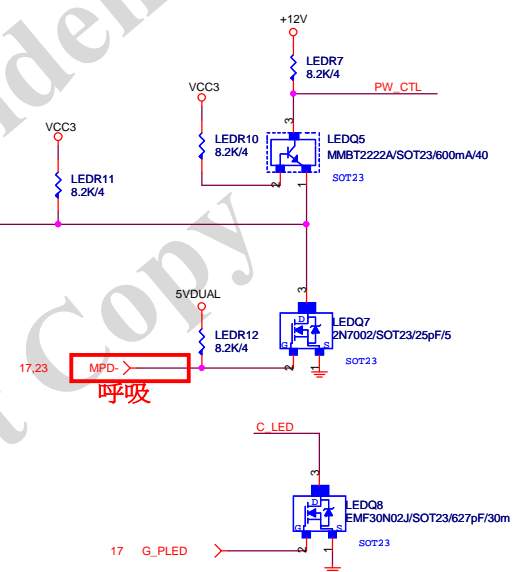
三色 LED Control

	IO_GP20(R)	IO_GP21(G)	IO_GP22(B)
Blue	L	L	H
Green	L	H	L
Light Blue	L	H	H
Red	H	L	L
Pink	H	L	H
Light Green	H	H	L
White	H	H	H
Cycle Mode	順序:Blue-Green-Light Blue-Red-Pink-Light Green-White 切换間隔時間為 1 秒		

- BOM OPTION :
- 1. YELLOW LED : LED/Y/6/M/S
 - 2. RED LED : LED/R/H/0603/S
 - 3. GREEN LED : LED/G/0603/S

Ambient LED Control

	IO_GP95	IO_GP91
Still Mode	H	L
OFF Mode	L	L
Pluse Mode	H	BREATH



呼吸

